Thomas Kattwinkel

8-bit microcontrollers SAB C504-2E and SAB C504-2R:

Accurate modulation of pulse width

The C504 microcontroller is a development of the C501 featuring a high-performance capture/compare unit. This new member of the Siemens 8-bit family allows three-phase asynchronous motors, or four, five and six-phase unipolar motors to be controlled with a resolution up to 50 ns.

Based on the C501 microcontroller with full 80C52 compatibility, the new C504* additionally features a self-calibrating 10-bit A/D converter with up to eight inputs, four each on ports 1 and 3 (**Fig. 1**). Another innovation allows the analog inputs to be used as digital outputs or inputs. The minimum conversion time is 6 µs at an oscillator frequency of 32 MHz. The C504 is equipped with a total of four 16-bit timers and one 10-bit timer, all implemented on-chip. Timers 0 to 2 are familiar from the earlier SAB 80C52. In addition, timer 2 allows the direction of counting to be reversed via an external pin (port 1.1). In comparison with the SAB 80C52, memory capacity has been doubled in the new microcontroller, which has 16K bytes of ROM and 512 bytes of RAM. Another new feature is the deactivation option for the ALE signal for single-chip mode.

Two extra compare timers

The additional capture/compare unit consists of compare timers 1 and 2 with resolutions of 16 and 10 bits respectively. The first comprises two timers, which can be mutually offset via a 16-bit register. The output signals at the ports of the capture/compare unit can thus be mutually offset in 2^{16} steps with a minimum resolution of 50 ns, so that a defined idle time can be set. The idle time can thus be set very precisely for a particular application in which a three-phase full bridge is driven, thus avoiding a temporary short circuit in the bridge.

If a specific period and a defined idle time are set with compare timer 1 and the offset timer, compare timer 2 can be used to modulate the pulse width of the duty factor set with compare timer 1. The capture/compare unit can be operated in both edge-aligned and center-aligned modes, so that the current controller can be directly implemented by means of compare timer 2 (burst mode). Compare timers 1 and 2 are each fitted with an eight-step prescaler that provides all the flexibility required for the various applications. The pulse pattern of compare timer 2 (with a variable period and duty factor) can additionally be made available as another compare output at the C OUT 3 pin.

The six output signals of the PWM unit can be assigned a defined level in the initialization phase (COINI bits). The C504 has a CTRAP input that can immediately apply PWM channels selectively to the level (inactive level) specified during initialization with COINI as soon as a low level is applied to the CTRAP pin. If this level changes back to high, all channels for which the CTRAP was cleared are again included in the pulse width modulation at the beginning of a new period. If a CTRAP occurs, the CPU is informed of this event by an interrupt, assuming this function is enabled. This allows the turn-off pattern for the six outputs to be selectively defined, for instance in the event of excess current in one of the three phases of an asynchronous motor.

A major advantage of this two-timer configuration becomes apparent when an asynchronous motor with sine-wave modulation is run up and switched over to trapezoidal operation after reaching a defined speed. In this case, compare timer 1 is used to set a specific period and a duty cycle of, say, 10%. To ensure smooth start-up of the motor, it must be possible to modulate the pulse of the duty cycle with a resolution of at least 10 bits during the period in which the break-

*See data sheets for complete type names (to PRO ELECTRON) of all microcontrollers mentioned here

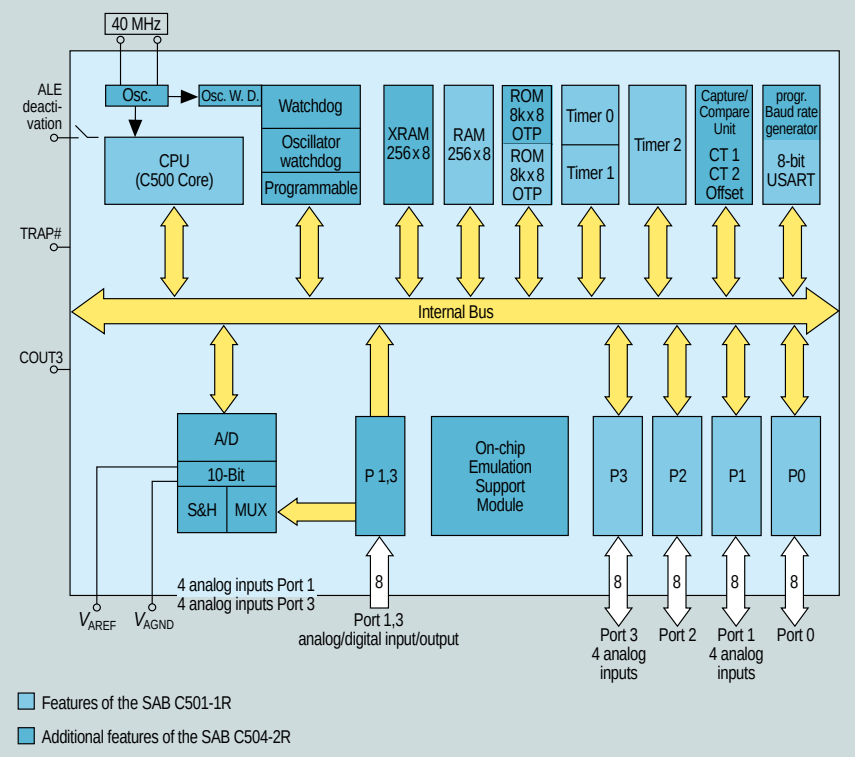

Fig. 1 The C504 is based on the C501, but has several extra features

loose moment must be overcome. This is the only way of attaining a sufficiently fine graduation of the various voltage stages to be specified. This capability in particular underlines the high performance of the C504.

Simple procedure for block commutation

The multichannel PWM mode of the capture/compare unit allows a permanently excited three-phase asynchronous motor, operated as a DC series machine, to be run in block commutating mode. Three Hall-effect sensors, placed at an angle that depends on the number of pole pairs on the stator, supply the commutation pattern. The signals from the Hall-effect sensors are transferred straight to the interrupt inputs INT 0 to INT 2. These can evaluate both positive and negative edges and in this mode generate the pulse pattern for the full bridge at CC 0 to CC 2 and C OUT 0 to C OUT 2 directly via a hardware-implemented table. Compare timer 2 acts as a current regulator. The signals from the Hall-effect sensors are checked for plausibility with reference to the pattern to be expected for the operating state. In the event of an implausible pattern, the capture/compare unit can be set to idle via an interrupt.

The same table can be used to operate four, five and six-phase unipolar motors very simply in another multichannel mode, in both clockwise and counterclockwise rotation (and with a lower software requirement).

Oscillator watchdog for fast power-on reset

The C504 is equipped with a programmable watchdog and an oscillator watchdog, which simultaneously performs the function of the fast power-on reset (defined port-pin level after a maximum of 34 µs). Internally, the clock of an RC oscillator, which runs up immediately after the supply voltage is applied, is set to a frequency comparator that permanently checks whether the quartz oscillator clock is oscillating at the nominal frequency. If so, the internal processor clock is switched over to the quartz oscillator – for reasons of safety after a delay – and the software execution can begin.

The watchdog control register WDCON can query the cause of a reset. When the watchdog timer status flag is set, it can be assumed that the watchdog was not operated during the time set (512 ms to 1.1 s at 12 MHz). If the status flag of the oscillator watchdog timer is set, the quartz oscillator clock failed at least temporarily. If none of the bits were set, a hardware reset occurred.

Another new performance feature is the wake-up function that allows the microcontroller to be reactivated from a software power-down via a low level at pin INT 0.

ROM protection has been implemented to protect proprietary rights. It can be optionally assigned during mask release. A ROM verification mode is also available to verify the system's own ROM code in steps of 16 bytes.

This component can be emulated by means of enhanced Hooks emulators. In this process, the ROM emulation is performed through each series component, so bond-out chips can be dispensed with. These performance features give the C504 a very good price/performance ratio for applications in the low-cost drives sector (e.g. in washing machines or dryers) and SPC controllers as well as in multiphase stepper motors and block-commutated motors. First samples of the C504 will be available in the second quarter of 1996, and an OTP version with optional read-out protection will be ready in the fourth quarter of 1996. It will be housed in an MQFP-44 package. h

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Thomas Kattwinkel, Dipl.-Ing.,

studied electrical engineering at Stuttgart University. Since 1989, Mr. Kattwinkel (36) has been working for the Semiconductor Group in Stuttgart as a field applications engineer for 8 and 16-bit microcontrollers.