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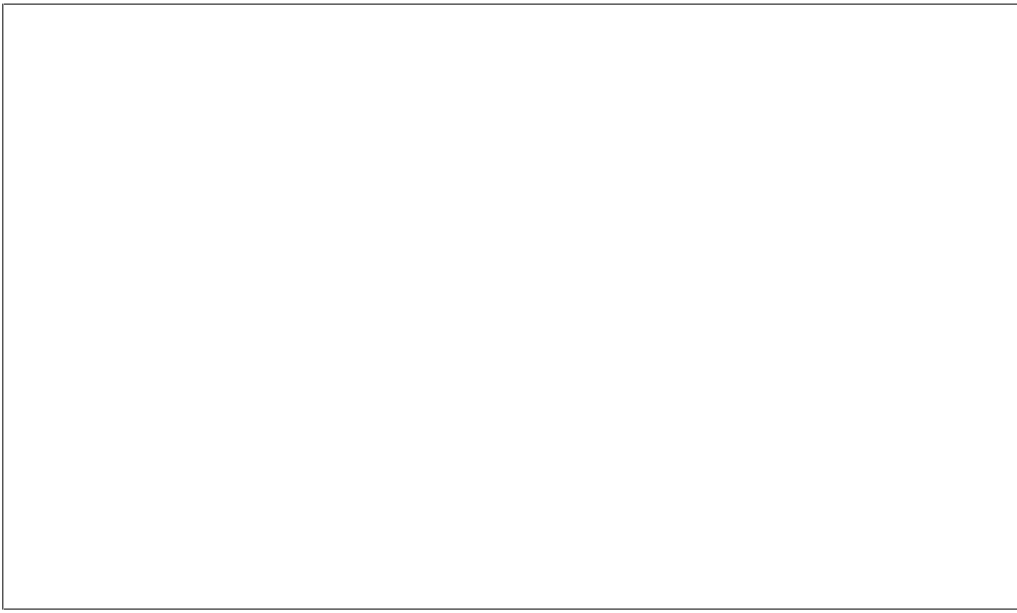

Microcomputer Components

SAB 80C515A / SAB 83C515A-5

8-Bit CMOS Microcontroller

Addendum to User’s Manual SAB 80515 / 80C515 08.95

SAB 80C515A/83C515A-5 Addendum **Revision History:** **Current Version: 08.95**	
Previous Version: **11.92**	
Page	Subjects (major changes since last revision)
3-6 3-16 5-4 5-10	CCH4 / CCL4 deleted Table supplemented (MOVX @Ri, $\overline{EA}$ = 1, 00) Falling edge for P4.0 / $\overline{ADST}$ in figure 5-2 added Formula for SREL added
6-1	New release of SAB 80C515A / 83C515A-5 data sheet inserted

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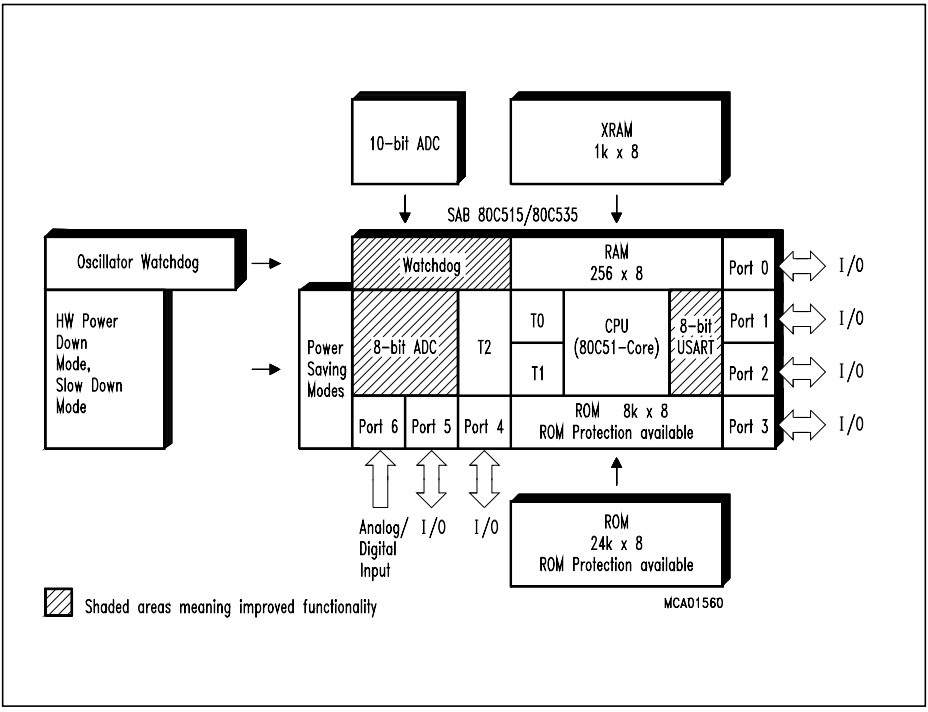
1 Introduction

The SAB 80C515A is a superset of the high end microcontroller SAB 80C515.

While maintaining all architectural and operational characteristics of the SAB 80C515 the SAB 80C515A incorporates more on-chip RAM. A new 10-bit A/D-Converter is implemented as well as an oscillator watchdog unit. Also the operating frequency is higher than at the SAB 80C515.



SAB 80C515A / 83C515A-5

The SAB 80C515A is available in two different versions:

- "ROMless" Version SAB 80C515A. Although this part is called "ROMless" there is an internal ROM of 2 KByte (for Test and Loader Software)
- ROM Version SAB 83C515A-5. This part has 32 KByte on-chip ROM.

With exception of the ROM sizes both parts are identical. Therefore the term SAB 80C515A refers to both versions within this specification unless otherwise noted.

This manual describes only the new features of the SAB 80C515A in addition to the features of the SAB 80C515/80C535. For reference to the SAB 80C515, the user's manual should be used.

Listed below is a summary of the main features of the SAB 80C515A:

- SAB 80C515A/83C515A-5, up to 18 MHz operation frequency
- 32 K × 8 ROM (SAB 83C515A-5 only, ROM-Protection available)
- 256 × 8 on-chip RAM
- additional 1 K × 8 on-chip RAM (XRAM)
- Superset of SAB 80C51 architecture:
  - 1 µs instruction cycle time at 12 MHz
  - 666 ns instruction cycle time at 18 MHz
  - 256 directly addressable bits
- Boolean processor
- 64 Kbyte external data and program memory addressing
- Three 16-bit timer/counters
- Versatile "fail-safe" provisions
- 12 interrupt vectors, four priority levels selectable
- genuine 10-bit A/D converter with 8 multiplexed inputs
- Full duplex serial interface with programmable Baudrate-Generator
- Functionally compatible with SAB 80C515
- Extended power saving modes
- Fast Power-On Reset
- Six ports: 48 I/O lines, 8 input lines
- Three temperature ranges available:
  0 to 70 °C (T1)
  – 40 to + 85 °C (T3)
  – 40 to + 110 °C (T4)
- Plastic package: P-LCC-68

The pin functions of the SAB 80C515A are identical with those of the SAB 80C515 with following exceptions:

	SAB 80C515A	SAB 80C515
Pin 68	$\overline{\text{HWPD}}$	V_{CC}
Pin 1	P4.0/$\overline{\text{ADST}}$	P4.0
Pin 4	$\overline{\text{PE}}$/SWD	$\overline{\text{PE}}$

2 Fundamental Structure

The SAB 80C515A/83C515A-5 is a high-end member of the Siemens SAB 8051 microcontroller family. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C515A/ 83C515A-5 contains more on-chip RAM/ROM. Furthermore a new 10-bit A/D-Converter is implemented as well as extended security mechanisms. The SAB 80C515A is identical with the SAB 83C515A-5 except that it lacks the on-chip program memory. The SAB 80C515A/ 83C515A-5 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).

The essential enhancements to the SAB 80C515 are (see also **figure 2-1**):

- Additional 1KByte RAM on chip
- 8-Channel 10-bit A/D Converter
- New baud rate generator for the Serial Channel
- Oscillator Watchdog Unit
- Improved functionality of the Watchdog Timer
- Hardware controlled Power Down Mode
- High speed operation of the device (up to 18 MHz crystal frequency)

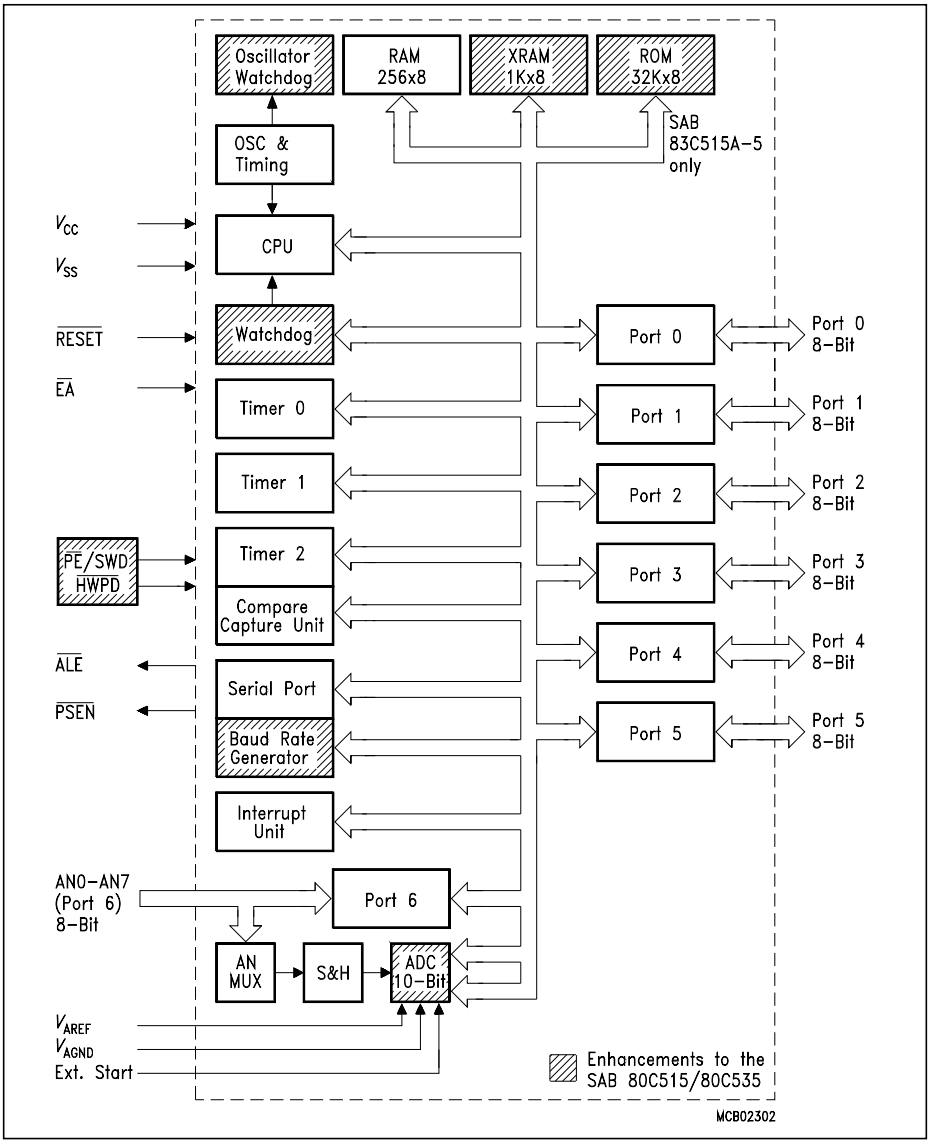


Figure 2-1
Block Diagram of the SAB 80C515A / 83C515A-5

3 Memory Organization

According to the SAB 8051 architecture, the SAB 80C515A has separate address spaces for program and data memory. **Figure 3-1** illustrates the mapping of address spaces.

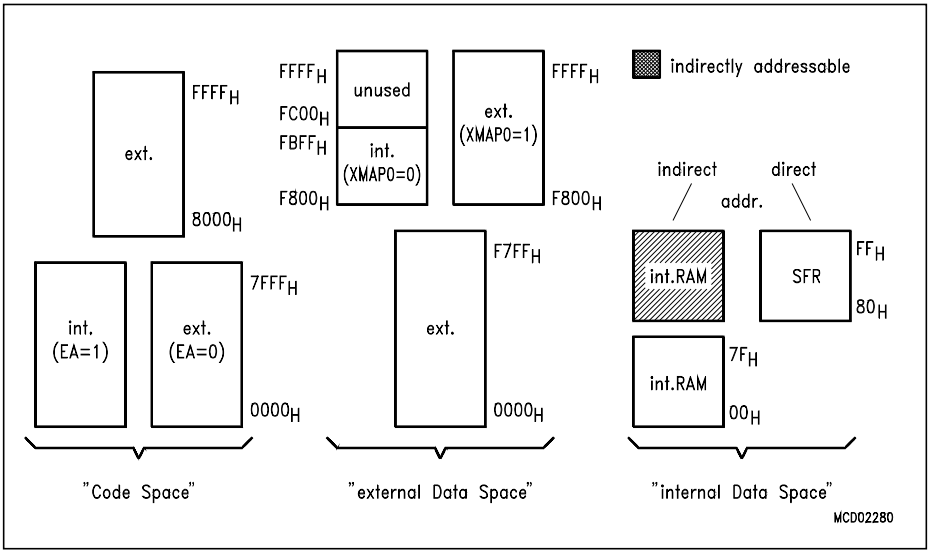


Figure 3-1
Memory Map

3.1 Program Memory, ROM Protection

The SAB 83C515A-5 has 32 Kbyte of on-chip ROM, while the SAB 80C515A has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin $\overline{EA}$ determines whether program fetches below address 8000H are done from internal or external memory.

As a new feature the SAB 83C515A-5 offers the possibility of protecting the internal ROM against unauthorized access. This protection is implemented in the ROM-Mask. Therefore, the decision ROM-Protection 'yes' or 'no' has to be made when delivering the ROM-Code. Once enabled, there is no way of disabling the ROM-Protection.

Effect: The access to internal ROM done by an externally fetched MOVC instruction is disabled. Nevertheless, an access from internal ROM to external ROM is possible.

To verify the read protected ROM-Code a special ROM-Verify-Mode is implemented. This mode also can be used to verify unprotected internal ROM.

ROM-Protection	**ROM-Verification Mode (see 'AC Characteristics')**	**Restrictions**
no	ROM-Verification Mode 1 (standard 8051 Verification Mode) ROM-Verification Mode 2	–
yes	ROM-Verification Mode 2	– standard 8051 Verification Mode is disabled – externally applied MOVC accessing internal ROM is disabled

3.2 Data Memory

The data memory space consists of an internal and an external memory space. The SAB 80C515A contains another 1 kByte of On-Chip RAM additional to the 256 Bytes internal RAM of the base type SAB 80C515. This RAM is called XRAM ('eXtended RAM') in this document.

- External Data Memory
  Up to 64 Kbyte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions in combination with registers R0 and R1 can be used. A 16-bit external memory addressing is supported by a 16-bit datapointer. Registers XPAGE and SYSCON are controlling whether data fetches at addresses $F800_H$ to $FBFF_H$ are done from internal XRAM or from external data memory.
- Internal Data Memory
  The internal data memory is divided into four physically distinct blocks:
  - the lower 128 bytes of RAM including four register banks containing eight registers each
  - the upper 128 byte of RAM
  - the 128 byte special function register area
  - a 1Kx8 area which is accessed like external RAM (MOVX-instructions), implemented on chip at the address range from $F800_H$ to $FBFF_H$. Special Function Register SYSCON controls whether data is read from or written to XRAM or external RAM.

3.3 Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area.
All special function registers are listed in **table 3-1** and **table 3-2**.

In **table 3-1** they are organized in numeric order of their addresses. In **table 3-2** they are organized in groups which refer to the functional blocks of the SAB 80C515A.

Table 3-1
Special Function Register

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	**P0** [1]	**FF_H**	**$A0_H$**	**P2** [1]	**FF_H**
81_H	SP	07_H	$A1_H$	reserved	XX_H [2]
82_H	DPL	00_H	$A2_H$	reserved	XX_H [2]
83_H	DPH	00_H	$A3_H$	reserved	XX_H [2]
84_H	(WDTL)		$A4_H$	reserved	XX_H [2]
85_H	(WDTH)		$A5_H$	reserved	XX_H [2]
86_H	WDTREL	00_H	$A6_H$	reserved	XX_H [2]
87_H	PCON	00_H	$A7_H$	reserved	XX_H [2]
88_H	**TCON** [1]	**00_H**	**$A8_H$**	**IEN0** [1]	**00_H**
89_H	TMOD	00_H	$A9_H$	IP0	00_H
$8A_H$	TL0	00_H	AA_H	SRELL	$0D9_H$
$8B_H$	TL1	00_H	AB_H	reserved	XX_H [2]
$8C_H$	TH0	00_H	AC_H	reserved	XX_H [2]
$8D_H$	TH1	00_H	AD_H	reserved	XX_H [2]
$8E_H$	reserved	XX_H [2]	AE_H	reserved	XX_H [2]
$8F_H$	reserved	XX_H [2]	AF_H	reserved	XX_H [2]
90_H	**P1** [1]	**FF_H**	**$B0_H$**	**P3** [1]	**FF_H**
91_H	XPAGE	00_H	$B1_H$	SYSCON	$XXXXXX01_B$ [2]
92_H	reserved	XX_H [2]	$B2_H$	reserved	XX_H [2]
93_H	reserved	XX_H [2]	$B3_H$	reserved	XX_H [2]
94_H	reserved	XX_H [2]	$B4_H$	reserved	XX_H [2]
95_H	reserved	XX_H [2]	$B5_H$	reserved	XX_H [2]
96_H	reserved	XX_H [2]	$B6_H$	reserved	XX_H [2]
97_H	reserved	XX_H [2]	$B7_H$	reserved	XX_H [2]
98_H	**SCON** [1]	**00_H**	**$B8_H$**	**IEN1** [1]	**00_H**
99_H	SBUF	XX_H [2]	$B9_H$	IP1	$XX000000_B$ [2]
$9A_H$	reserved	XX_H [2]	BA_H	SRELH	$XXXXXX11_B$ [2]
$9B_H$	reserved	XX_H [2]	BB_H	reserved	XX_H [2]
$9C_H$	reserved	XX_H [2]	BC_H	reserved	XX_H [2]
$9D_H$	reserved	XX_H [2]	BD_H	reserved	XX_H [2]
$9E_H$	reserved	XX_H [2]	BE_H	reserved	XX_H [2]
$9F_H$	reserved	XX_H [2]	BF_H	reserved	XX_H [2]

1) Bit-addressable Special Function Register

2) X means that the value is indeterminate and the location is reserved

Table 3-1, Special Function Register (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$C0_H$	**IRCON** [1]	**00_H**	**$E0_H$**	**ACC** [1]	**00_H**
$C1_H$	CCEN	00_H	$E1_H$	reserved	XX_H [2]
$C2_H$	CCL1	00_H	$E2_H$	reserved	XX_H [2]
$C3_H$	CCH1	00_H	$E3_H$	reserved	XX_H [2]
$C4_H$	CCL2	00_H	$E4_H$	reserved	XX_H [2]
$C5_H$	CCH2	00_H	$E5_H$	reserved	XX_H [2]
$C6_H$	CCL3	00_H	$E6_H$	reserved	XX_H [2]
$C7_H$	CCH3	00_H	$E7_H$	reserved	XX_H [2]
$C8_H$	**T2CON** [1]	**00_H**	**$E8_H$**	**P4** [1]	**FF_H**
$C9_H$	reserved	XX_H [2]	$E9_H$	reserved	XX_H [2]
CA_H	CRCL	00_H	EA_H	reserved	XX_H [2]
CB_H	CRCH	00_H	EB_H	reserved	XX_H [2]
CC_H	TL2	00_H	EC_H	reserved	XX_H [2]
CD_H	TH2	00_H	ED_H	reserved	XX_H [2]
CE_H	reserved	XX_H [2]	EE_H	reserved	XX_H [2]
CF_H	reserved	XX_H [2]	EF_H	reserved	XX_H [2]
$D0_H$	**PSW** [1]	**00_H**	**$F0_H$**	**B** [1]	**00_H**
$D1_H$	reserved	XX_H [2]	$F1_H$	reserved	XX_H [2]
$D2_H$	reserved	XX_H [2]	$F2_H$	reserved	XX_H [2]
$D3_H$	reserved	XX_H [2]	$F3_H$	reserved	XX_H [2]
$D4_H$	reserved	XX_H [2]	$F4_H$	reserved	XX_H [2]
$D5_H$	reserved	XX_H [2]	$F5_H$	reserved	XX_H [2]
$D6_H$	reserved	XX_H [2]	$F6_H$	reserved	XX_H [2]
$D7_H$	reserved	XX_H [2]	$F7_H$	reserved	XX_H [2]
$D8_H$	**ADCON0** [1]	**00_H**	**$F8_H$**	**P5** [1]	**FF_H**
$D9_H$	ADDATH	00_H	$F9_H$	reserved	XX_H [2]
DA_H	ADDATL	00_H	FA_H	reserved	XX_H [2]
DB_H	P6	XX_H [2]	FB_H		
DC_H	ADCON1	$XXXX0000_B$ [2]	FC_H		
DD_H	reserved	XX_H [2]	FD_H		
DE_H	reserved	XX_H [2]	FE_H		
DF_H	reserved	XX_H [2]	FF_H		

1) Bit-addressable Special Function Register

2) X means that the value is indeterminate and the location is reserved

Table 3-2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	$0D0_H$ [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	$0DC_H$	$0XXX\ 0000_B$ [3]
	ADDATH	A/D Converter Data Register High Byte	$0D9_H$	00_H
	ADDATL	A/D Converter Data Register Low Byte	$0DA_H$	00_H
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0	Interrupt Priority Register 0	$0A9_H$	00_H
	IP1	Interrupt Priority Register 1	$0B9_H$	$XX00\ 0000_B$ [3]
	IRCON	Interrupt Request Control Register	**$C0_H$** [1]	00_H
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	00_H
Compare/ Capture-Unit (CCU)	CCEN	Comp./Capture Enable Reg.	$0C1_H$	00_H
	CCH1	Comp./Capture Reg. 1, High Byte	$0C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$0C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$0C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$0C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$0C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$0C6_H$	00_H
	CRCH	Com./Rel./Capt. Reg. High Byte	$0CB_H$	00_H
	CRCL	Com./Rel./Capt. Reg. Low Byte	$0CA_H$	00_H
	TH2	Timer 2, High Byte	$0CD_H$	00_H
	TL2	Timer 2, Low Byte	$0CC_H$	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
XRAM	XPAGE	Page Addr. Reg. for extended onchip RAM	91_H	00_H
	SYSCON	XRAM Control Reg.	$0B1_H$	$XXXX\ XX01_B$ [3]

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

Table 3-2, Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	$0FF_H$
	P1	Port 1	**90_H** 1	$0FF_H$
	P2	Port 2	**$A0_H$** 1)	$0FF_H$
	P3	Port 3	**$B0_H$** 1)	$0FF_H$
	P4	Port 4	**$E8_H$** 1)	$0FF_H$
	P5	Port 5	**$F8_H$** 1)	$0FF_H$
	P6	Port 6, Analog/Digital Input	DB_H	
Power Save Modes	PCON	Power Control Register	87_H	00_H
Serial Channels	ADCON0 2)	A/D Converter Control Reg.	**$0D8_H$** 1)	00_H
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Reg.	99_H	$0XX_H$ 3)
	SCON	Serial Channel Control Reg.	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Reg., low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Reg., high byte	BA_H	XXXX $XX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Watchdog	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
	IP1 2)	Interrupt Priority Register 1	$B9_H$	XX00 0000_B 3)
	WDTREL	Watchdog Timer Reload Reg.	86_H	00_H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is indeterminate and the location is reserved

3.4 Architecture of the XRAM.

The contents of the XRAM is not affected by a reset or HW Power Down. After power-up the contents is undefined, while it remains unchanged during and after a reset or HW Power Down if the power supply is not turned off.

The additional On-Chip RAM is logically located in the "external data memory" range at the upper end of the 64 KByte address range ($F800_H$ -$FBFF_H$). Nevertheless when XRAM is enabled the address range $F800_H$ to $FFFF_H$ is occupied. This is done to assure software compatibility to SAB 80C517A. It is possible to enable and disable (only by reset) the XRAM. If it is disabled the device shows the same behaviour as the parts without XRAM, i.e. all MOVX accesses use the external bus to physically external data memory.

3.4.1 Accesses to XRAM

Because the XRAM is used in the same way as external data memory the same instruction types must be used for accessing the XRAM.

Note:

If a reset occurs during a write operation to XRAM, the effect on XRAM depends on the cycle which the reset is detected at (MOVX is a 2-cycle instruction):

Reset detection at cycle 1: The new value will not be written to XRAM. The old value is not affected.

Reset detection at cycle 2: The old value in XRAM is overwritten by the new value.

Accesses to XRAM using the DPTR

There are a Read and a Write instruction from and to XRAM which use one of the 16-bit DPTR for indirect addressing. The instructions are:

```
MOVX    A, @DPTR    (Read)
MOVX    @DPTR, A    (Write)
```

Normally the use of these instructions would use a physically external memory. However, in the SAB 80C515A the XRAM is accessed if it is enabled and if the DPTR points to the XRAM address space (DPTR $\geq F800_H$).

Accesses to XRAM using the Registers R0/R1

The 8051 architecture provides also instructions for accesses to external data memory range which use only an 8-bit address (indirect addressing with registers R0 or R1). The instructions are:

MOVX	A, @ Ri	(Read)
MOVX	@Ri, A	(Write)

In application systems, either a real 8-bit bus (with 8-bit address) is used or Port 2 serves as page register which selects pages of 256-Byte. However, the distinction, whether Port 2 is used as general purpose I/0 or as "page address" is made by the external system design. From the device's point of view it cannot be decided whether the Port 2 data is used externally as address or as I/0 data!

Hence, a special page register is implemented into the SAB 80C515A to provide the possibility of accessing the XRAM also with the MOVX @Ri instructions, i.e. XPAGE serves the same function for the XRAM as Port 2 for external data memory.

Special Function Register XPAGE

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr.91H									XPAGE

The reset value of XPAGE is 00_H.

XPAGE can be set and read by software.

Figures 3-2 to **3-4** show the dependencies of XPAGE- and Port 2 - addressing in order to explain the differences in accessing XRAM, ext. RAM or what is to do when Port 2 is used as an I/O-port.

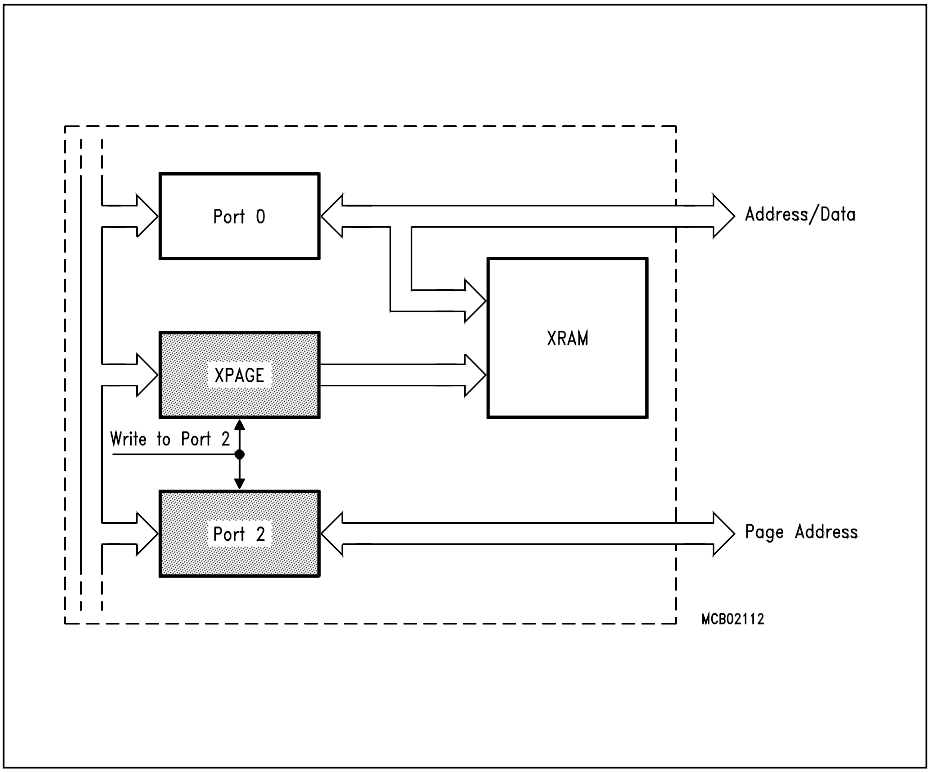


Figure 3-2
Write Page Address to Port 2

MOV P2, pageaddress will write the page address to Port 2 **and** XPAGE-Register.

When external RAM is to be accessed in the XRAM address range ($F800_H$ - $FFFF_H$) XRAM has to be disabled. When additional external RAM is to be addressed in an address range ≤ XRAM ($F800_H$) XRAM may remain being enabled and there is no need to overwrite XPAGE by a second move.

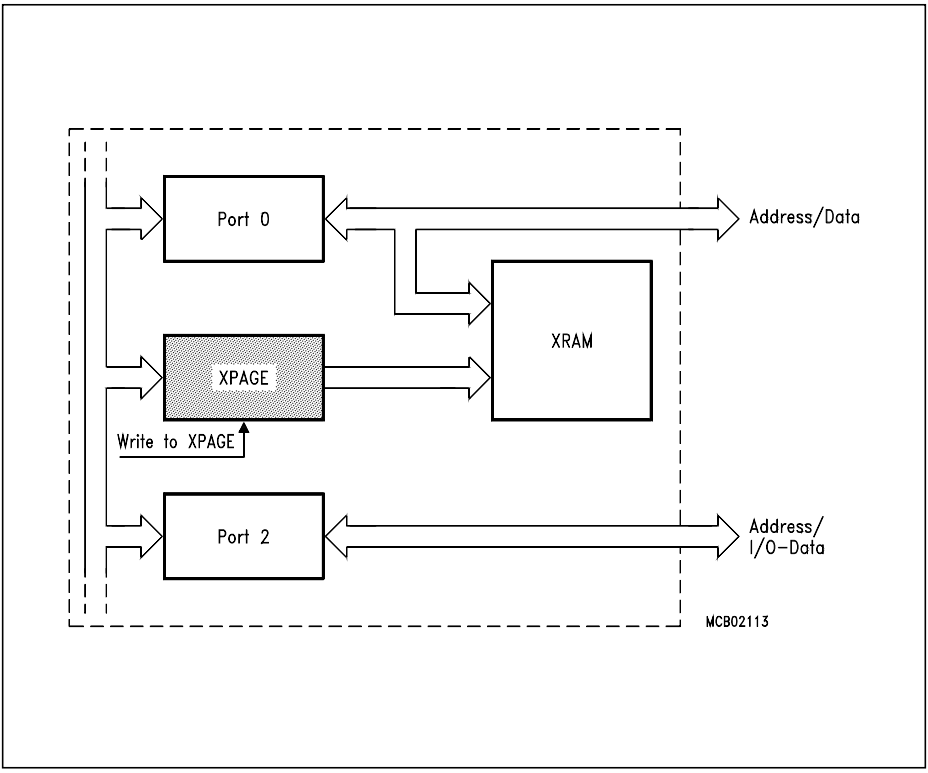


Figure 3-3
Write Page Address to XPAGE

The page address is only written to XPAGE-register. Port 2 is available for addresses or I/O-Data. See **figure 3-4** to see what happens when Port 2 is used as I/O-Port.

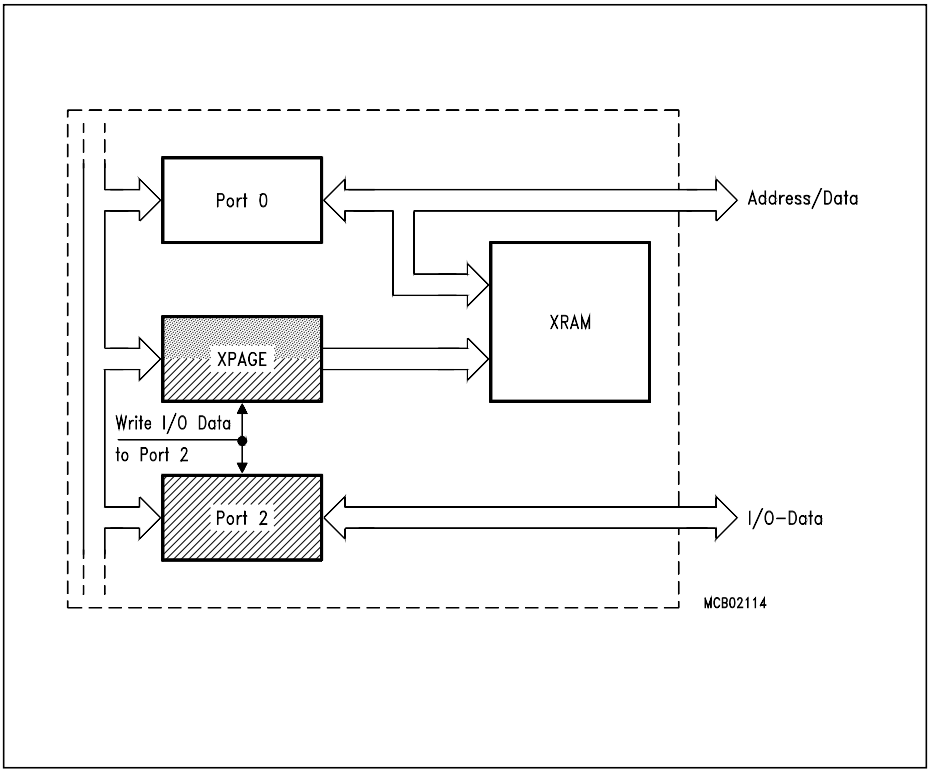


Figure 3-4
Use of Port 2 as I/O-Port

At a write to Port 2, XRAM address in XPAGE-register will be overwritten because of the concurrent write to Port 2 and XPAGE-register. So whenever XRAM is used and the XRAM address differs from the byte written to Port 2 latch it is absolutely necessary to rewrite XPAGE with page address.

Example:

I/O-Data at Port 2 shall be $0AA_H$. A Byte shall be fetched from XRAM at address $0F830_H$

```
MOV R0, #30H
MOV P2, #0AAH       ; P2 shows 0AAH
MOV XPAGE, #0F8H    ; P2 still shows 0AAH but XRAM is addressed
MOVX A, @R0         ; the contents of XRAM at 0F830H is moved to accu
```

The register XPAGE provides the upper address byte for accesses to XRAM with MOVX @Ri instructions. If the address formed from XPAGE and Ri is less than the XRAM address range, then an external access is performed. For the SAB 80C515A the contents of XPAGE must be greater or equal than F8H in order to use the XRAM. Of course, the XRAM must be enabled if it shall be used with MOVX @Ri instructions.

Thus, the register XPAGE is used for addressing of the XRAM; additionally its contents are used for generating the internal XRAM select. If the contents of XPAGE is less than the XRAM address range then an external bus access is performed where the upper address byte is provided by P2 and not by XPAGE!

Therefore, the software has to distinguish two cases, if the MOVX @Ri instructions with paging shall be used:

a) Access to XRAM: The upper address byte must be written to XPAGE or P2; both writes selects the XRAM address range.

b) Access to external memory: The upper address byte must be written to P2; XPAGE will be loaded with the same address in order to deselect the XRAM.

The behaviour of Port0, Port2 and the $\overline{RD}$/$\overline{WR}$ signals depends on the state of pin $\overline{EA}$ and on the control bits XMAP0 and XMAP1 in register SYSCON.

3.4.2 Control of XRAM in the SAB 80C515A

There are two control bits in register SYSCON which control the use and the bus operation during accesses to the additional On-Chip RAM in XDATA range (≙XRAM).

Special Function Register SYSCON

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr.0B1$_H$	–	–	–	–	–	–	XMAP1	XMAP0	SYSCON

Bit	Function
XMAP0	Global enable/disable bit for XRAM memory. XMAP0 = 0: The access to XRAM (= On-Chip XDATA memory) is enabled. XMAP0 = 1: The access to RAM is disabled. All MOVX accesses are performed by the external bus. This bit is hardware protected.
XMAP1	Control bit for $\overline{RD}$/$\overline{WR}$ signals during accesses to XRAM; this bit has no effect if XRAM is disabled (XMAP0 = 1) or if addresses outside the XRAM address range are used for MOVX accesses. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to XRAM. XMAP1 = 1: Ports 0, 2 and the signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM.

Reset value of SYSCON is XXXX XX01$_B$.

The control bit XMAP0 is a global enable/disable bit for the additional On-Chip RAM (XRAM). If this bit is set, the XRAM is disabled, all MOVX accesses use external memory via the external bus. In this case the SAB 80C515A can't use the additional On-Chip RAM and is compatible with the types without XRAM.

A hardware protection is done by an unsymmetric latch at XMAP0-bit. A unintentional disabling of XRAM could be dangerous since indeterminate values could be read from external bus. To avoid this the XMAP-bit is forced to '1' only by reset. Additional during reset an internal capacitor is loaded. So the reset state is a disabled XRAM. Because of the load time of the capacitor XMAP0-bit once written to '0' (that is, discharging capacitor) cannot be set to '1' again by software. On the other hand any distortion (software hang up, noise,...) is not able to load this capacitor, too. That is, the stable status is XRAM enabled. The only way to disable XRAM after it was enabled is a reset.

The clear instruction for the XMAP0-bit should be integrated in the program initialization routine before XRAM is used. In extremely noisy systems the user may have redundant clear instructions.

The control bit XMAP1 is relevant only if the XRAM is accessed. In this case the external $\overline{RD}$ and $\overline{WR}$ signals at P3.6 and P3.7 are not activated during the access, if XMAP1 is cleared. For debug purposes it might be useful to have these signals and the Ports 0, 2 available. This is performed if XMAP1 is set.

3.4.3 Behaviour of Port0 and Port2

The behaviour of Port 0 and P2 during a MOVX access depends on the control bits in register SYSCON and on the state of pin $\overline{EA}$. The **table 3-3** lists the various operating conditions. It shows the following characteristics:

a) Use of P0 and P2 pins during the MOVX access.
   Bus: The pins work as external address/data bus. If (internal) XRAM is accessed, the data written to the XRAM can be seen on the bus in debug mode.
   I/0: The pins work as Input/Output lines under control of their latch.
b) Activation of the $\overline{RD}$ and $\overline{WR}$ pin during the access.
c) Use of internal or external XDATA memory.

The shaded areas describe the standard operation as each 80C51 device without on-chip XRAM behaves.

		$\overline{EA}$ = 0			$\overline{EA}$ = 1		
		XMAP1, XMAP0			**XMAP1, XMAP0**		
		00	**10**	**X1**	**00**	**10**	**X1**
MOVX @DPTR	DPTR < XRAM address range	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used
	DPTR ≥ XRAM address range	a)P0/P2→Bus ($\overline{WR}$-Data only) b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0/P2→Bus ($\overline{WR}$-Data only) b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c) ext.memory is used	a)P0/P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0/P2→Bus ($\overline{WR}$-Data only) b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0/P2→Bus b)$\overline{RD}$/$\overline{WR}$ active c) ext.memory is used
MOVX @ Ri	XPAGE < XRAM addr.page range	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used
	XPAGE ≥ XRAM addr.page range	a)P0→Bus ($\overline{WR}$-Data only) P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0→Bus ($\overline{WR}$-Data only) P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used	a)P2→I/O P0/P2→I/O b)$\overline{RD}$/$\overline{WR}$ inactive c)XRAM is used	a)P0→Bus ($\overline{WR}$-Data only) P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)XRAM is used	a)P0→Bus P2→I/O b)$\overline{RD}$/$\overline{WR}$ active c)ext.memory is used

(shaded) modes compatible to 8051-family

Table 3-3
Behaviour of P0/P2 and RD/WR During MOVX Accesses

4 System Reset

4.1 Additional Hardware Power Down Mode in the SAB 80C515A

The SAB 80C515A has an additional Power Down Mode which can be initiated by an external signal at a dedicated pin. This pin is labeled $\overline{\text{HWPD}}$ and is a floating input line (active low). This pin substitutes one of the V_{CC} pins of the base types SAB 80C515 (PLCC68: Pin68). Because this new power down mode is activated by an external hardware signal this mode is referred to as Hardware Power Down Mode in opposite to the program controlled Software Power Down Mode.

Pin $\overline{\text{PE}}$/SWD has no control function for the Hardware Power Down Mode; it enables and disables only the use of all software controlled power saving modes (Idle Mode, Software Power Down Mode).

The function of the new Hardware Power Down Mode is as follows:

The pin $\overline{\text{HWPD}}$ controls this mode. If it is on logic high level (inactive) the part is running in the normal operating modes. If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the Hardware Power Down Mode; as mentioned above this is independent of the state of pin $\overline{\text{PE}}$/SWD.

$\overline{\text{HWPD}}$ is sampled once per machine cycle. If it is found active, the device starts a complete internal reset sequence. This takes two machine cycles; all pins have their default reset states during this time. This reset has exactly the same effects as a hardware reset; i.e.especially the watchdog timer is stopped and its status flag WDTS is cleared. In this phase the power consumption is not yet reduced. After completion of the internal reset both oscillators of the chip are disabled, the on-chip oscillator as well as the oscillator watchdog's RC oscillator. At the same time the port pins and several control lines enter a floating state as shown in **table 4-1**. In this state the power consumption is reduced to the power down current I_{PD}. Also the supply voltage can be reduced. **Table 4-1** also lists the voltages which may be applied at the pins during Hardware Power Down Mode without affecting the low power consumption.

Table 4-1
Status of all Pins During Hardware Power Down Mode

Pins	Status	Voltage Range at Pin During HW-Power Down
P0, P1, P2, P3, P4, P5, P6	Floating outputs/ Disabled input function	$V_{SS} \le V_{IN} \le V_{CC}$
$\overline{EA}$	Active input	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
$\overline{PE}$/SWD	Active input, Pull-up resistor Disabled during HW power down	$V_{IN} = V_{CC}$ or $V_{IN} = V_{SS}$
XTAL 1	Active output	pin may not be driven
XTAL 2	Disabled input function	$V_{SS} \le V_{IN} \le V_{CC}$
$\overline{PSEN}$, ALE	Floating outputs/ Disabled input function (for test modes only)	$V_{SS} \le V_{IN} \le V_{CC}$
$\overline{Reset}$	Active input; must be at high level if HWPD is used	$V_{IN} = V_{CC}$
V_{AREF}	ADC reference supply input	$V_{SS} \le V_{IN} \le V_{CC}$

The power down state is maintained while pin $\overline{\text{HWPD}}$ is held active. If HWPD goes to high level (inactive state) an automatic start up procedure is performed:

- First the pins leave their floating condition and enter their default reset state as they had immediately before going to float state.
- Both oscillators are enabled. While the on-chip oscillator (with pins XTAL1 and XTAL2) usually needs a longer time for start-up, if not externally driven (with crystal approx. 1 ms), the oscillator watchdog's RC oscillator has a very short start-up time (typ. less than 2 microseconds).
- Because the oscillator watchdog is active it detects a failure condition if the on-chip oscillator hasn't yet started. Hence, the watchdog keeps the part in reset and supplies the internal clock from the RC oscillator.
- Finally, when the on-chip oscillator has started, the oscillator watchdog releases the part from reset after it performed a final internal reset sequence and switches the clock supply to the on-chip oscillator. This is exactly the same procedure as when the oscillator watchdog detects first a failure and then a recovering of the oscillator during normal operation. Therefore, also the oscillator watchdog status flag is set after restart from Hardware Power Down Mode.
  When automatic start of the watchdog was enabled ($\overline{\text{PE}}$/SWD connected to V_{CC}), the Watchdog Timer will start, too (with its default reload value for time-out period).

The SWD-Function of the $\overline{\text{PE}}$/SWD Pin is sampled only by a hardware reset.Therefore at least one Power On Reset has to be performed.

4.2 Hardware Power Down Reset Timing

Following figures are showing the timing diagrams for entering (**figure 4-1**) and leaving (**figure 4-2**) the Hardware Power Down Mode. If there is only a short signal at pin $\overline{\text{HWPD}}$ (i.e. $\overline{\text{HWPD}}$ is sampled active only once), then a complete internal reset is executed. Afterwards the normal program execution starts again (**figure 4-3**).

Note:

Delay time caused by internal logic is not included.

The $\overline{\text{Reset}}$ pin overrides the Hardware Power Down function, i.e. if reset gets active during Hardware Power Down it is terminated and the device performs the normal reset function. Thus, pin $\overline{\text{Reset}}$ has to be inactive during Hardware Power Down Mode.

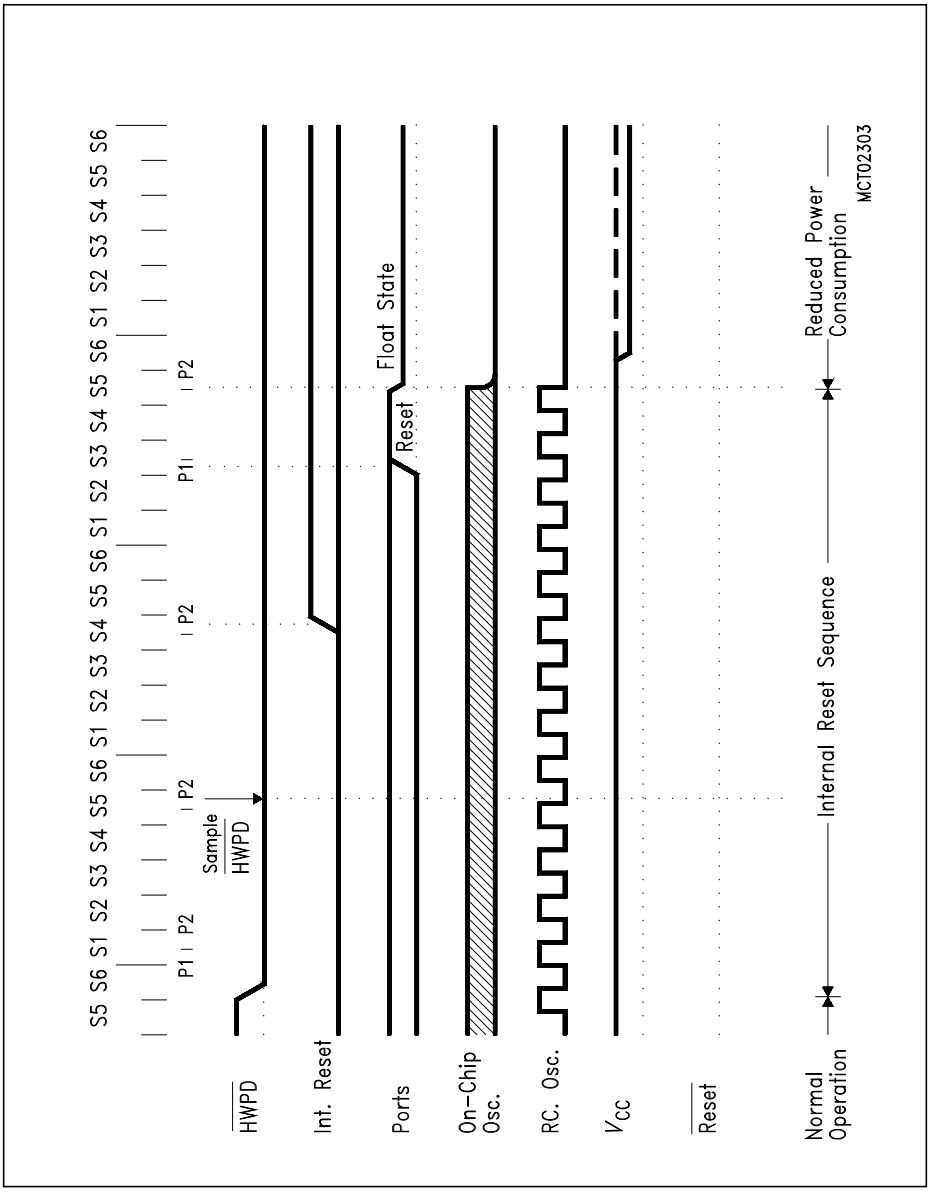


Figure 4-1
Timing Diagram of Entering Hardware Power Down Mode

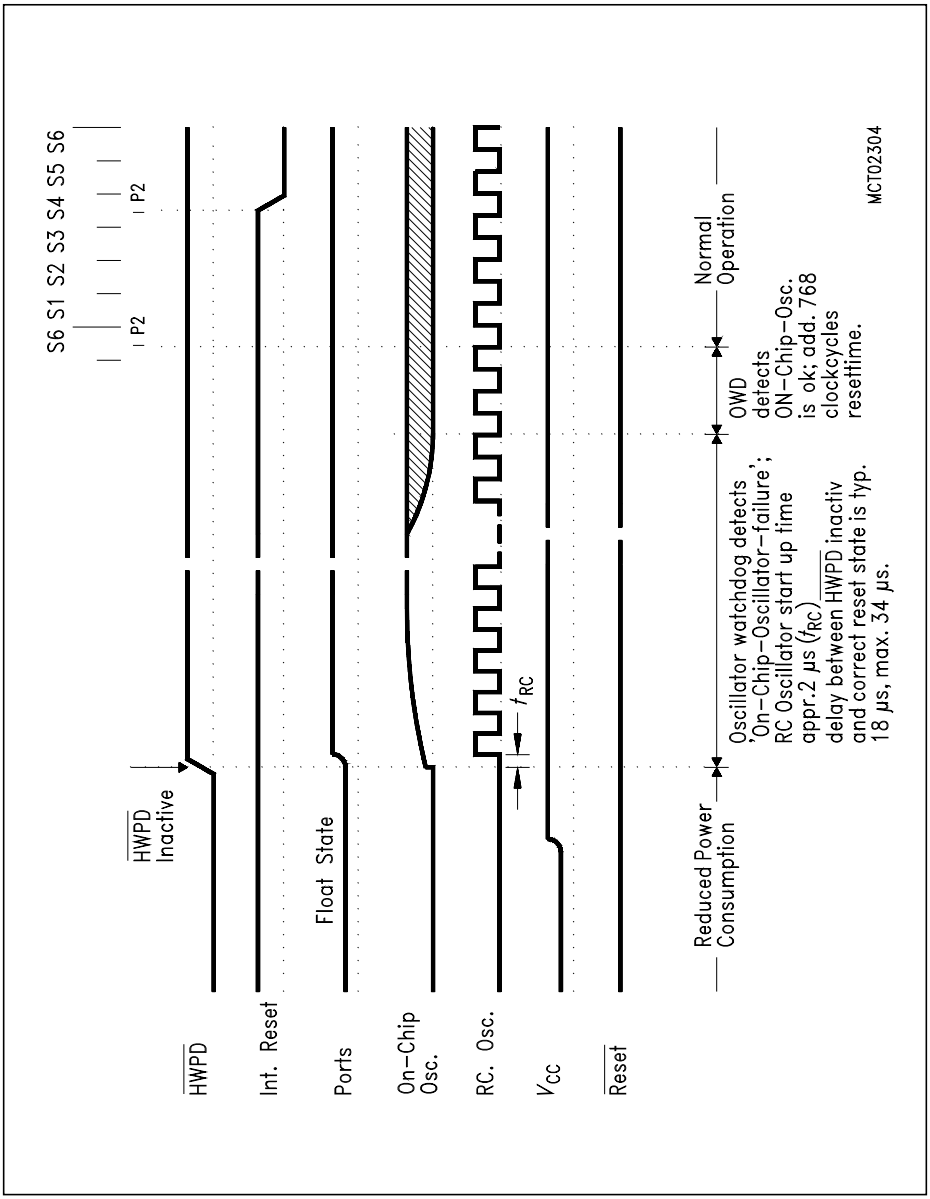


Figure 4-2
Timing Diagram of Leaving Hardware Power Down Mode

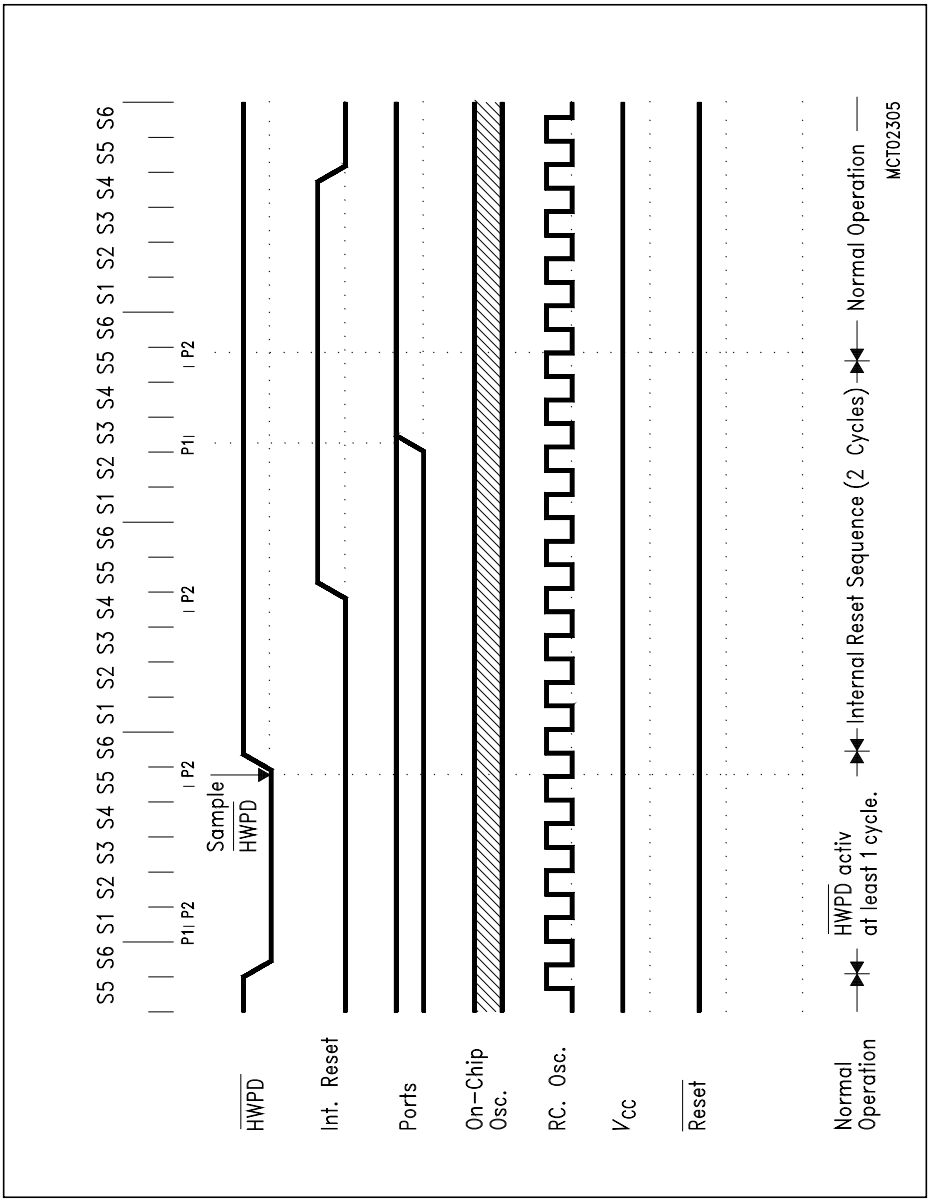


Figure 4-3
Timing Diagram of Hardware Power Down Mode, $\overline{\text{HWPD}}$-Pin is active for only one Cycle

4.3 Fast Internal Reset after Power-On

The SAB 80C515A can use the oscillator watchdog unit for a fast internal reset procedure after power-on.

Figure 4-4 shows the power-on sequence under control of the oscillator watchdog.

Normally the devices of the 8051 family (like the SAB 80C515) enter their default reset state not before the on-chip oscillator starts. The reason is that the external reset signal must be internally synchronized and processed in order to bring the device into the correct reset state. Especially if a crystal is used the start up time of the oscillator is relatively long (typ. 1ms). During this time period the pins have an undefined state which could have severe effects especially to actuators connected to port pins.

In the SAB 80C515A the oscillator watchdog unit can avoid this situation. In this case, after power-on the oscillator watchdog's RC oscillator starts working within a very short start-up time (typ. less than 2 microseconds). In the following the watchdog circuitry detects a failure condition for the on-chip oscillator because this has not yet started (a failure is always recognized if the watchdog's RC oscillator runs faster than the on-chip oscillator). As long as this condition is detected the watchdog uses the RC oscillator output as clock source for the chip rather than the on-chip oscillator's output. This allows correct resetting of the part and brings also all ports to the defined state (see **figure 4-4**). The time period from power-on until reaching the reset state at the ports derives from the following terms:

- RC oscillator start-up < 2 µs
- synchronization of the RC oscillators divider-by-5 < 6T
- synchronization of the state and cycle counters < 6T
- reset procedure till correct port states are reached < 12T

Delay between power-on and correct reset state:

Typ: 18 µs
Max.: 34 µs

After the on-chip oscillator finally has started, the oscillator watchdog detects the correct function; then the watchdog still holds the reset active for a time period of 768 cycles of the RC oscillator in order to allow the oscillation of the on-chip oscillator to stabilize (**figure 4-4**, II). Subsequently the clock is supplied by the on-chip oscillator and the oscillator watchdog's reset request is released (**figure 4-4**, III). However, an externally applied reset still remains active (**figure 4-4**, IV) and the device does not start program execution (**figure 4-4**, V) before the external reset is also released.

Although the oscillator watchdog provides a fast internal reset it is additionally necessary to apply the external reset signal when powering up. The reasons are as follows:

- Termination of Hardware Power Down Mode (a $\overline{\text{HWPD}}$ signal is overridden by reset)
- Termination of Software Power Down Mode
- Reset of the status flag OWDS that is set by the oscillator watchdog during the power up sequence.

The external reset signal must be hold active at least until the on-chip oscillator has started and the internal watchdog reset phase is completed. An external reset time of more than 50 µs should be sufficient in typical applications. If only a capacitor at pin $\overline{\text{Reset}}$ is used a value of less than 100 nF provides the desired reset time.

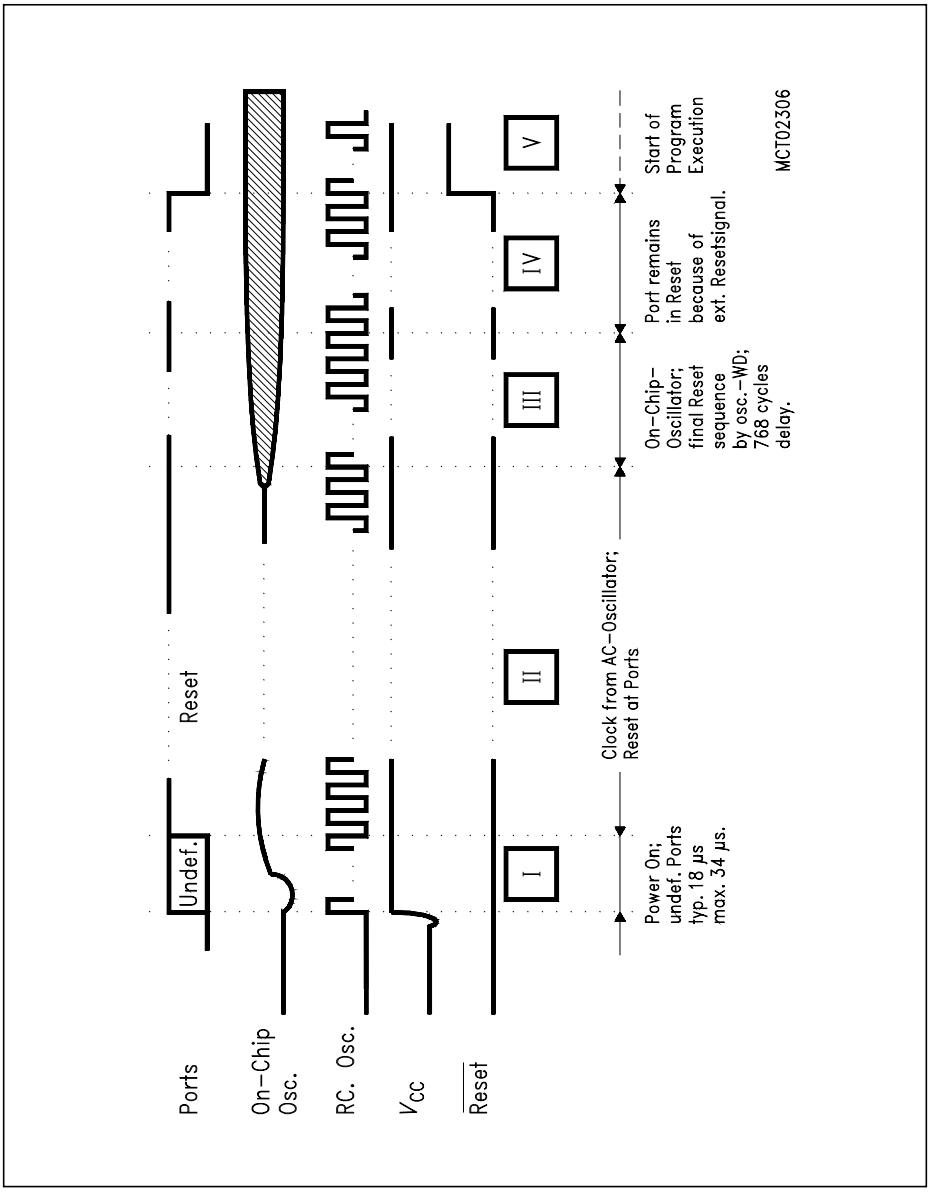


Figure 4-4
Power-on of the SAB 80C515A

5 On-Chip Peripheral Components

Digital I/O Port Circuitry

To realize the Hardware Power Down Mode with floating Port pins in the SAB 80C515A/83C515A-5 the standard port structure used in the 8051 Family is modified (**figure 5-1**).

The FETs p4, p5 and n2 are added. During Hardware Power Down this FETs disconnect the port pins from internal logic.

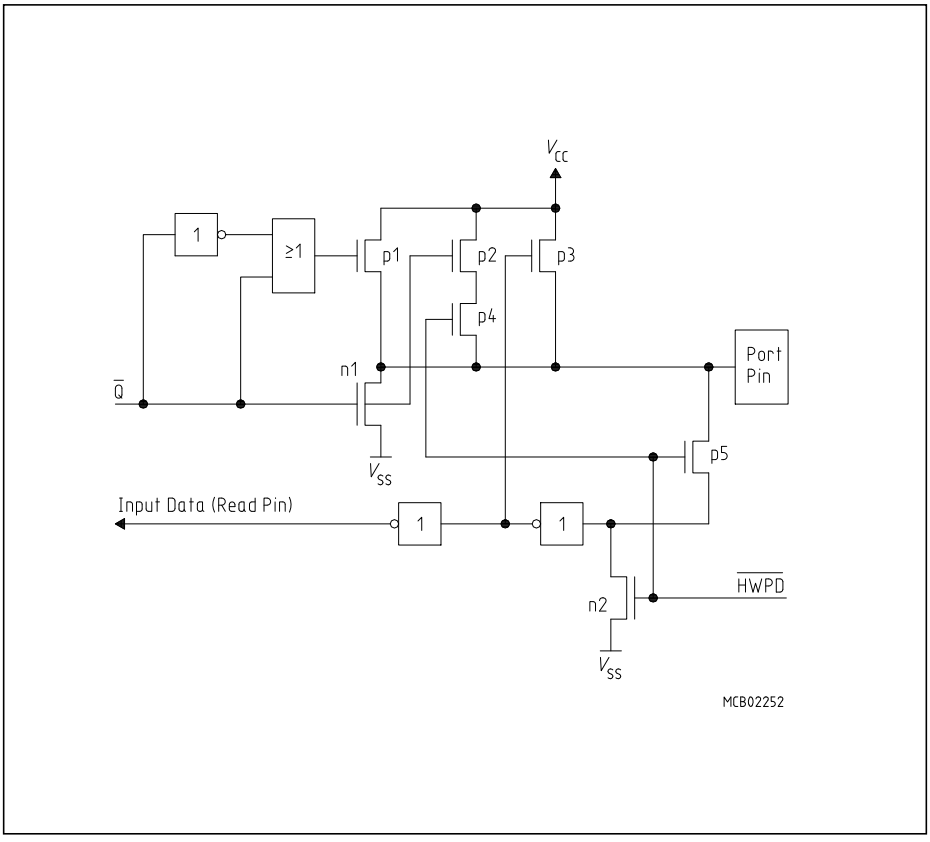


Figure 5-1
Port Structure

P1 and p3 are not active during Hardware Power Down.

P1 is activated only for two oscillator periods if a 0-to-1 transition is programmed to the port pin (not possible during HWPD).

P3 is turned off during reset state (also HWPD).

For detailed description of the port structure please refer to the SAB 80C515/80C535 User's Manual.

5.1 10-Bit A/D-Converter

In the SAB 80C515A a new high performance/high speed 8-channel 10-bit A/D-Converter is implemented. Its successive approximation technique provides 7 µs conversion time (f_{OSC} = 16 MHz). The conversion principle is upward compatible to the one used in the SAB 80C515. The major components are shown in **figure 5-1**.

The comparator is a fully differential comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted providing 10-bit resolution.

The table below shows the sample time T_S and the conversion time T_C (including T_S), which depend on f_{OSC} and the selected prescaler (see also Bit ADCL in SFR ADCON 1).

f_{osc} [MHz]	Prescaler	f_{ADC} [MHz]	T_S [µs]	T_C [µs] (incl. T_S)
12	÷ 8	1.5	2.67	9.33
	÷ 16	0.75	5.33	18.66
16	÷ 8	2.0	2.0	7.0
	÷ 16	1.0	4.0	14.0
18	÷ 8	–	–	–
	÷ 16	1.125	3.555	12.4

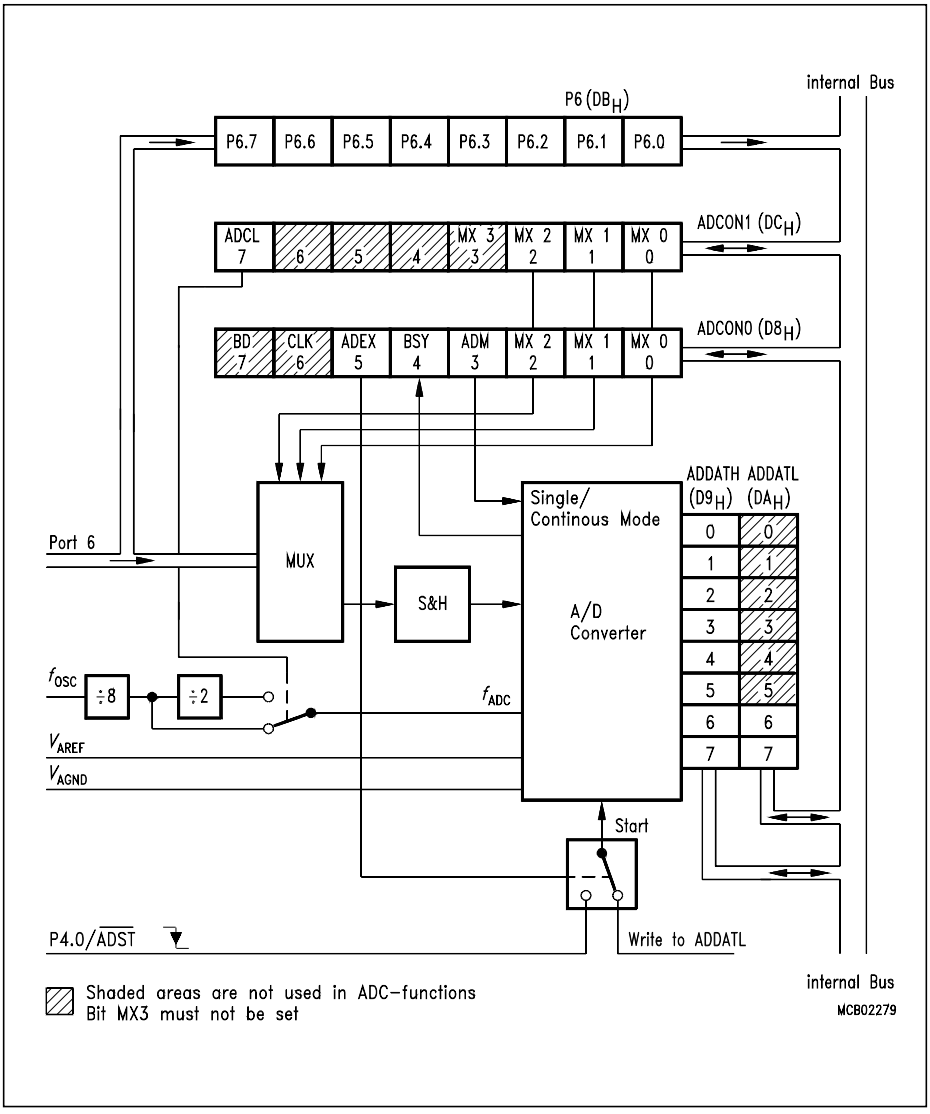


Figure 5-2
10-Bit A/D-Converter

Special Function Registers ADCON0, ADCON1

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $0D8_H$	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0	ADCON0

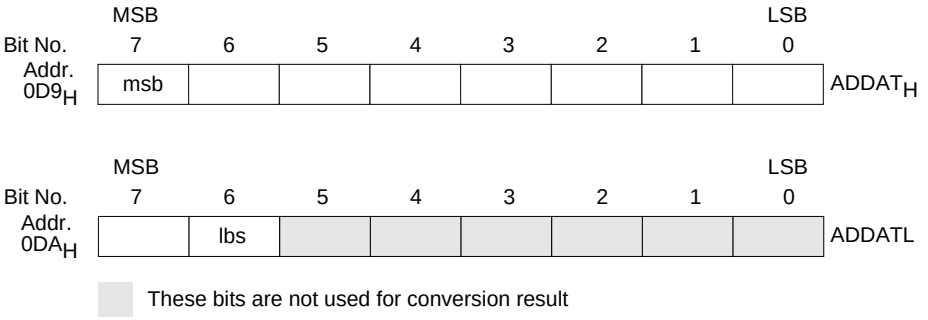
	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $0DC_H$	ADCL				MX3	MX2	MX1	MX0	ADCON1

These bits are not used in controling A/D converter functions in the 80C515A

Bit	Function
ADEX	Internal/external start of conversion. When set, the external start of conversion by P4.0 / $\overline{ADST}$ is enabled
BSY	Busy flag. This flag indicates whether a conversion is in progress (BSY = 1). The flag is cleared by hardware when the conversion is finished.
ADM	A/D Conversion mode. When set, a continuous conversion is selected. If cleared, the converter stops after one conversion.
MX2 - MX0	Select 8 input channels of the ADC. Bits MX0 to MX2 can be written or read either in ADCON0 or in ADCON1
ADCL	ADC Clock. When set $f_{ADC} = f_{OSC} / 16$. Has to be set when $f_{OSC} > 16$ MHz

The reset value of ADCON0 and ADCON1 is 00_H

Special Function Register ADDATH, ADDATL



The reset value of $ADDAT_H$ and ADDATL is 00_H.

The registers **$ADDAT_H$** ($0D9_H$) and **ADDATL** ($0DA_H$) contain the 10-bit conversion result. The data is read as two 8-bit bytes. Data is presented in left justified format (i.e. the msb is the most left-hand bit in a 16-bit word). To get a 10-bit conversion result two READ operations are required. Otherwise $ADDAT_H$ contains the 8-bit conversion result.

A/D Converter Timing

After a conversion has been started (by a write to ADDATL, external start by P4.0/$\overline{\text{ADST}}$ or in continuous mode) the analog input voltage is sampled for 4 clock cycles. The analog source must be capable of charging the capacitor network of appr. 50 pF to full accuracy in this time. During this period the converter is susceptable to spikes and noise at the analog input, which may cause wrong codes at the digital outputs. Therefore RC-filtering at the analog inputs is recommended (see figure below).

Conversion of the sampled analog voltage takes place between the 4th an 14th clock cycle.

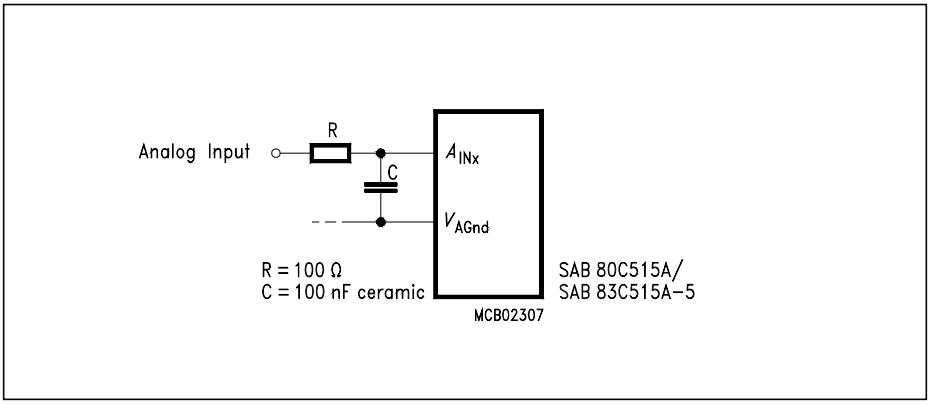


Figure 5-3
Recommended RC-Filtering at the Analog Inputs

5.2 New Baud Rate Generator for Serial Channel

The Serial Channel has a new baud rate generator which provides greater flexibility and better resolution. It substitutes the 80C515's baud rate generator at the Serial Channel which provides only 4.8 kBaud or 9.6 kBaud at 12 MHz crystal frequency. Since the new generator offers greater flexibility it is often possible to use it instead of Timer1 which is then free for other tasks.

Figure 5-3 shows a block diagram of the new baud rate generator for the Serial Channel. It consists of a free running 10-bit timer with f_{OSC} / 2 input frequency. On overflow of this timer there is an automatic reload from the registers SRELL (address AA_H) and SRELH (address BA_H). The lower 8 bits of the timer are reloaded from SRELL, while the upper two bits are reloaded from bit 0 and 1 of register SRELH. The baud rate timer is reloaded by writing to SRELL.

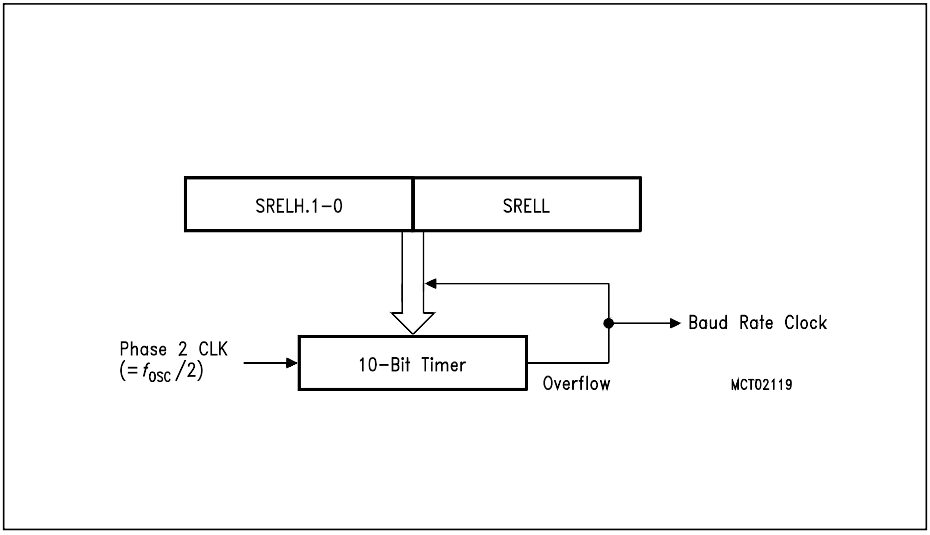
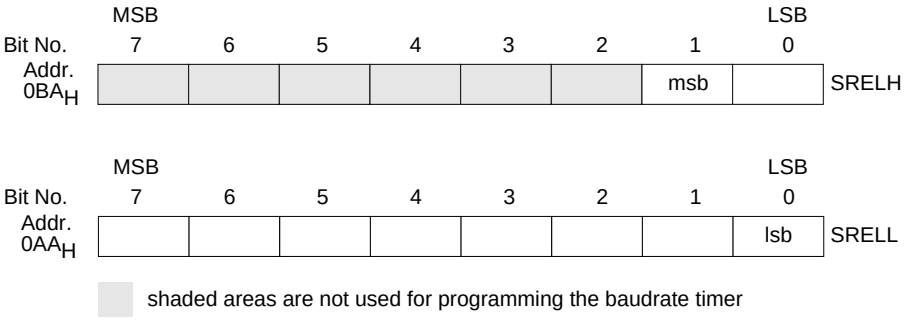


Figure 5-4
Baud Rate Generator for the Serial Interface

Special Function Register S0RELH, S0RELL



Bit	Function
SRELH.0-1	Reload value. Upper two bits of the timer reload value.
SRELL.0-7	Reload value. Lower 8 bit of timer reload value.

Reset value of SRELL is $0D9_H$, SRELH contains XXXX $XX11_B$.

Figure 5-5 shows a block diagram of the options available for baud rate generation of Serial Channel. It is a fully compatible superset of the functionality of the SAB 80C515. The new baud rate generator can be used in modes 1 and 3 of the Serial Channel. It is activated by setting bit BD (ADCON.7). This also starts the baud rate timer. When Timer1 shall be used for baud rate generation, bit BD must be cleared. In any case, bit SMOD (PCON.7) selects an additional divider by two.

The default values after reset in registers SRELL and SRELH provide a baud rate of 4.8 kBaud (with SMOD = 0) or 9.6 kBaud (with SMOD = 1) at 12 MHz oscillator frequency. This guarantees full compatibility to the SAB 80C515.

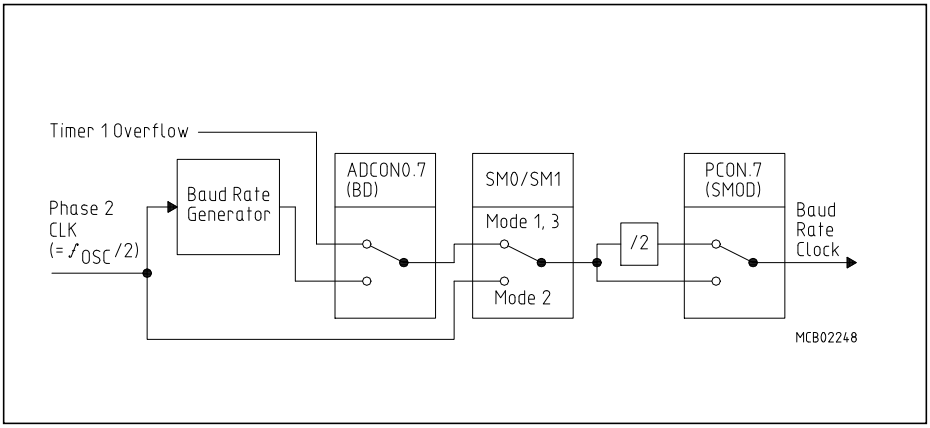


Figure 5-5
Block Diagram of Baud Rate Generation for Serial Interface

If the new baud rate generator is used the baud rate of the Serial Channel in Mode 1 and 3 can be determined as follows:

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times \text{oscillator frequency}}{64 \times (2^{10} - \text{SREL})}\ ; \text{with SREL = SRELH.1 – 0, SRELL.7 – 0}$$

$$\text{SREL} = 2^{10} - \frac{2^{SMOD} \times f_{OSC}}{64 \times \text{baud rate}}$$

5.3 Fail Save Mechanisms

The SAB 80C515A offers two on-chip peripherals which ensure an automatic 'fail-save' reaction in cases where the controller's hardware fails or the software hangs up:

- Programmable Watchdog Timer (WDT) with variable time-out period from 512 µs to approx. 1.1 seconds at 12 MHz. The SAB 80C515A's WDT is compatible to the SAB 80C515's WDT, which is not programmable.
- An Oscillator Watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into the reset state if the on-chip oscillator fails. This unit is new in with respect to the SAB 80C515.

5.3.1 Programmable Watchdog Timer

To protect the system against software upset, the user's program has to clear the watchdog within a previously programmed time period. If the software fails to do this periodical refresh of the Watchdog Timer, an internal hardware reset will be initiated. The software can be designed such that the watchdog times the if the program does not work properly. It also times out if a software error is based on hardware-related problems.

The Watchdog Timer in the SAB 80C515A is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). That is, the machine clock is divided by a series of arrangement of two prescalers, a divide-by-two and a divide-by-16 prescaler (**see figure 5-6**). The latter is enabled by setting bit WDTREL.7.

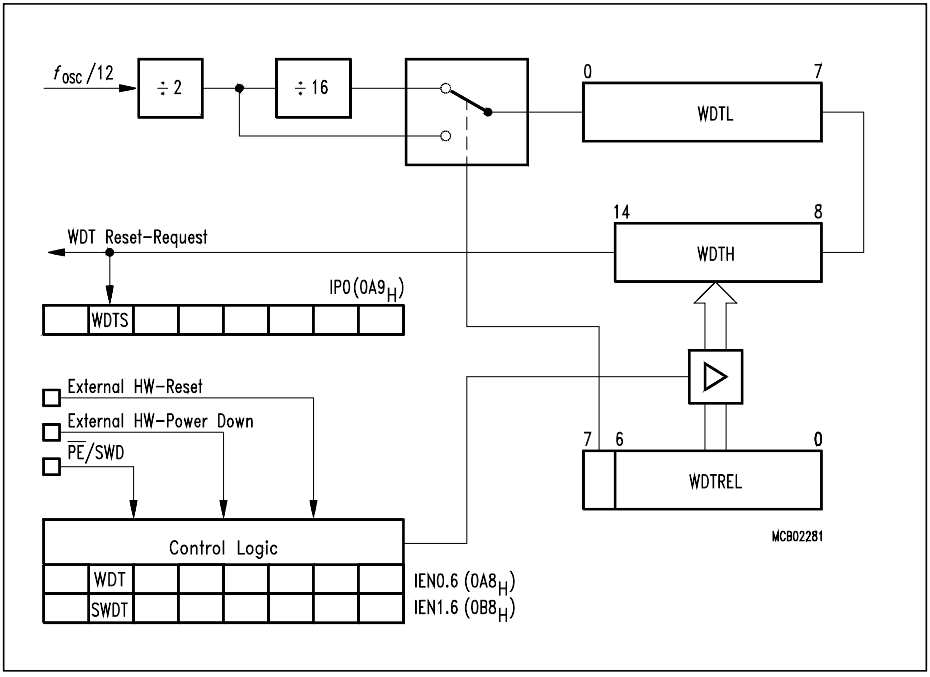
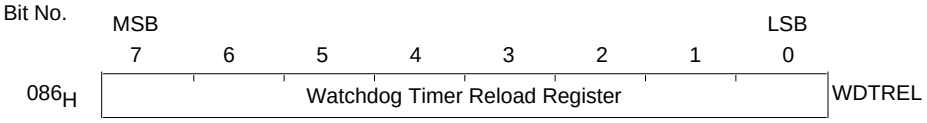


Figure 5-6
Block Diagram of the Programmable Watchdog Timer

Special Function Register WDTREL (Address 086_H)



Bit	Function
WDTREL.7	Prescaler select bit. When set, the watchdog timer is clocked through an additional divide-by-16 prescaler (see figure 12).
WDTREL.6 to WDTREL.0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

Reset value of WDTREL is 00_H.

Immediately after start (see next section for start procedure), the Watchdog Timer is initialized to the reload value programmed to WDTREL.0-WDTREL.6. After an external HW reset (or power-on reset, or HW Power Down) register WDTREL is cleared to 00_H. The lower seven bits of WDTREL can be loaded by software at any time.

Examples (given for 12 and 18 MHz oscillator frequency):

WDTREL	Time-out Period		Comments
	f_{osc} = 12 MHz	f_{osc} = 18 MHz	
00_H	65.535 ms	43.690 ms	This is the default value and coincides with the watchdog period of the SAB 80C515
80_H	1.1 s	0.73 s	maximum time period
$7F_H$	512 µs	341 µs	minimum time period

Starting the Watchdog Timer

There are two ways to start the Watchdog Timer depending on the level applied to the pin $\overline{PE}$/SWD (Power Down Modes enable # / Start Watchdog Timer; pin 4). This pin serves two functions (new for the SAB 80C515A), because it is also used for disabling the software initiated power saving modes. For details concerning software initiated power saving modes see User's Manual SAB 80C515.

Automatic Start of the Watchdog Timer

The automatic start of the Watchdog Timer directly after an external reset or a Hardware Power Down ($\overline{HWPD}$; PLCC68 pin 60, new for SAB 80C515A) is a hardware start initialized by strapping pin 4 ($\overline{PE}$/SWD) to V_{CC}. In this case the power saving modes (Software power-down mode and idle mode) are disabled and cannot be started by software. If pin $\overline{PE}$/SWD is left unconnected, a weak pull-up transistor ensures the automatic start of the Watchdog Timer.

The self-start of the Watchdog Timer by a pin option has been implemented to provide high system security in electrically noisy environments.

Note:

The automatic start of the Watchdog Timer is only performed if $\overline{PE}$/SWD is held at high level while $\overline{RESET}$ or $\overline{HWPD}$ is active. A positive transition at these pins during normal program execution will not start the Watchdog Timer.

Furthermore, when using the hardware start, the Watchdog Timer starts running with its default time-out period. The value in the reload register WDTREL, however can be overwritten at any time to set any time-out period desired.

Software Start of the Watchdog Timer

The Watchdog Timer can also be started by software. This method is compatible to the start procedure in the SAB 80C515. Setting of bit SWDT in SFR IEN1 starts the Watchdog Timer. Using the software start, the time-out period can be programmed before Watchdog Timer starts running.

Note that once started the Watchdog Timer cannot be stopped by anything but an external hardware reset at pin 10 ($\overline{RESET}$) with a low level on pin 4 ($\overline{PE}$/SWD) or a hardware power down at pin 60 ($\overline{HWPD}$, independently of level at $\overline{PE}$/SWD).

Refreshing the Watchdog Timer

At the same time the Watchdog Timer is started, the 7-bit register WDTH is preset by the contents of WDTREL.0 to WDTREL.6. Once started the Watchdog Timer cannot be stopped by software but can be refreshed to the reload value only by first setting bit WDT (IEN0.6) and by the next instruction setting SWDT (IEN1.6). Bit WDT will automatically be cleared during the second machine cycle after having been set [1]. This double-instruction refresh of the Watchdog Timer is implemented to minimize the chance of an unintentional reset of the watchdog unit.

The reload register WDTREL can be written at any time, as already mentioned. Therefore, a periodical refresh of WDTREL can be added to the above mentioned starting procedure of the Watchdog Timer. Thus a wrong reload value caused by a possible distortion during the write operation to WDTREL can be corrected by software.

Watchdog Reset and Watchdog Status Flag (WDTS)

If the software fails to clear the watchdog in time, an internally generated watchdog reset is entered at the counter state 7FFCH. The duration of the reset signal then depends on the prescaler selection (either 8 or 128 cycles). This internal reset differs from an external one in so far as the Watchdog Timer is not disabled and bit WDTS is set. Figure 5-6 shows a block diagram of all reset requests in the SAB 80C515A and the function of the watchdog status flag. The WDTS is a flip-flop, which is set by a Watchdog Timer reset and can be cleared by an external hardware reset. Bit WDTS allows the software to examine from which source the reset was activated. The bit WDTS can also be cleared by software.

[1] (SETB - Instructions have to be used)

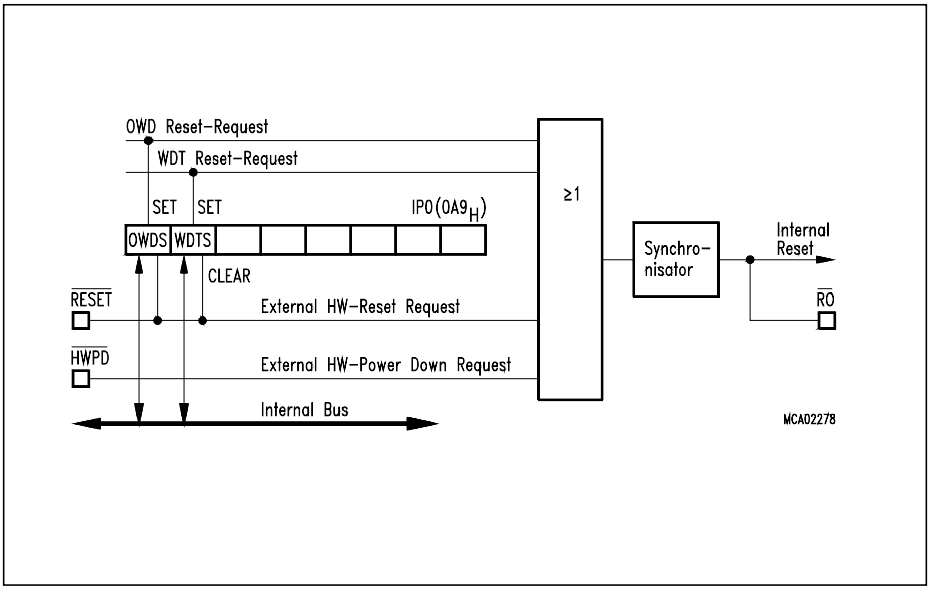


Figure 5-7
Watchdog Status Flags and Reset Requests

Special Function Register IP0 (Address $0A9_H$)

Bit No.

	MSB							LSB	
	7	6	5	4	3	2	1	0	
086_H	OWDS	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	IP0

These bits are not used for Watchdog Timer

Bit	Function
WDTS	Watchdog timer status flag. Set by hardware e when a Watchdog Timer reset occurred. Can be cleared and set by software.

Reset value of IP0 is 00_H.

5.3.2 Oscillator Watchdog Unit

The unit serves three functions:

- **Monitoring of the on-chip oscillator's function.**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of appr. 0.5 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Restart from the Hardware Power Down Mode.**
  If the Hardware Power Down Mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete Hardware Power Down sequence; however, the watchdog works identically to the monitoring function. The Hardware Power Down Mode is discussed in detail in section 4.1, 4.2
- **Fast internal reset after power-on.**
  In this function the oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. In this case the oscillator watchdog unit also works identically to the monitoring function. The power-on is described in section 4.3.

Note:

The oscillator watchdog unit is always enabled.

Detailed Description of the Oscillator Watchdog Unit

Figure 5-8 shows the block diagram of the oscillator watchdog unit. It consists of an internal RC oscillator which provides the reference frequency for the comparison with the frequency of the on-chip oscillator.

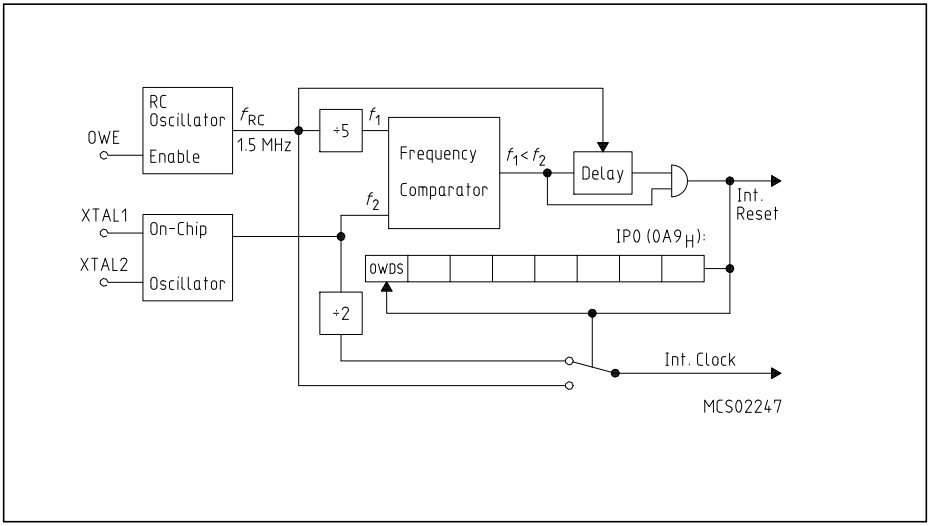


Figure 5-8
Oscillator Watchdog Unit

Special Function Register IP0 (Address 0A9$_H$)

Bit No.

	MSB 7	6	5	4	3	2	1	LSB 0	
086$_H$	OWDS	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	IPO

These bits are not used for Watchdog Timer

Bit	Function
OWDS	Oscillator watchdog timer status flag. Set by hardware when an oscillator watchdog reset occurred. Can be cleared and set by software.

Reset value of IP0 is 00$_H$.

The frequency coming from the RC oscillator is divided by 5 and compared to the on-chip oscillator's frequency. If the frequency coming from the on-chip oscillator is found lower than the frequency derived from the RC oscillator the watchdog detects a failure condition (the oscillation at the on-chip oscillator could stop because of crystal damage etc.). In this case it switches the input of the internal clock system to the output of the RC oscillator. This means that the part is being clocked even if the on-chip oscillator has stopped or has not yet started. At the same time the watchdog activates the internal reset in order to bring the part in its defined reset state. The reset is performed because clock is available from the RC oscillator. This internal watchdog reset has the same effects as an externally applied reset signal with the following exceptions: The Watchdog Timer Status flag WDTS (IP0.6) is not reset; (the Watchdog Timer however is stopped) and bit OWDS is set. This allows the software to examine error conditions detected by the Watchdog Timer even if meanwhile an oscillator failure occurred.

The oscillator watchdog is able to detect a recovery of the on-chip oscillator after a failure. If the frequency derived from the on-chip oscillator is again higher than the reference the watchdog starts a final reset sequence which takes typ. 1 ms. Within that time the clock is still supplied by the RC oscillator and the part is held in reset. This allows a reliable stabilization of the on chip oscillator. After that, the watchdog toggles the clock supply back to the on-chip oscillator and releases the reset request. If no external reset is applied in this moment the part will start program execution. If an external reset is active, however, the device will keep the reset state until also the external reset request disappears.

Furthermore, the status flag OWDS (IP0.7) is set if the oscillator watchdog was active. The status flag can be evaluated by software to detect that a reset was caused by the oscillator watchdog. The flag OWDS can be set or cleared by software. An external reset request, however, also resets OWDS (and WDTS).