SIEMENS

C500 Family

Member of C500 Family	max. Clock Rate (MHz)	ROM (KByte)	RAM (Byte) + XRAM (Byte)	I/O Lines	ADC-Inputs / Resolution	Timer/Counter (16-Bit)	Interrupt Vectors/Levels	Serial I/O	Full CAN Interface 2.0B active	PWM (Channels)	MDU	Data Pointers (16-Bit)	Hardware Power Down	Watchdog Timer	Osc Watchdog	Packaging	
C501-L / -1R	40	– / 8	256	32	–	3	6 / 2	USART	–	–	–	1	–	–	–	P-DIP-40 P-LCC-44 P-MQFP-44	Fully Compatible with 80C52/C32 Standard
C502-L / -2R	20	– / 16	256 + 256	32	–	3	6 / 2	USART	–	–	–	8	–			P-DIP-40 P-LCC-44	Prog. XRAM Start Address
C504-L / -2R*	40	– / 16	256 + 256	32	8 / 10	4	12 / 2	USART	–	6	–	1	–			P-MQFP-44	CCU for DC Motor Control
C511-R C511A-R	12	2,5 4	128 256	32	–	2	4 / 2	SSC	–	–	–	1	–	–	–	P-LCC-44	Low Power, Low EMC
C513-1R C513A-L / -R / -2R	12	8 – / 12 / 16	256 256 + 256	32	–	3	7 / 2	USART + SSC	–	–	–	1	–	–	–	P-LCC-44 P-MQFP-44	Low Power/EMC E^2PROM Version
C515-L / -1R	20	– / 8	256	56	Prog. Ref. 8 / 8	3	12 / 4	USART	–	4	–	1	–		–	P-MQFP-80	Compatible with SAB 80C515
C515B-2R* C515A-L / -4R*	20	16 – / 32	256 + 256 256 + 1K	56	8 / 10	3	12 / 4	USART	–	4	–	1				P-MQFP-80	Compatible with SAB 80C515A
C515C-8R*	10 [1]	64	256 + 2K	57	8 / 10	3	15 / 4	USART + SSC		4	–	8				P-MQFP-80	FCAN, Low EMC/Power
C517A-L / -4R*	20	– / 32	256 + 2K	68	12 / 10	4	17 / 4	USART + UART	–	21		8				P-MQFP-100	Compatible with SAB 80C517A
C509-L	16 [1]	–	256 + 3K	80	15 / 10	5	19 / 4	USART + UART	–	29		8				P-MQFP-100	CMOS/TTL Ports Bootstrap
SAB 80C535 SAB 80C515	20	– 8	256	56	Prog. Ref. 8 / 8	3	12 / 4	USART	–	4	–	1	–		–	P-LCC-68 P-MQFP-80	
SAB 80C515A SAB 83C515A-5	18	– 32	256 + 1K	56	8 / 10	3	12 / 4	USART	–	4	–	1				P-LCC-68 P-MQFP-80	
SAB 80C537 SAB 80C517	16	– 8	256	68	Prog. Ref. 12 / 8	4	14 / 4	USART + UART	–	21		8	–			P-LCC-84	
SAB 80C517A SAB 83C517A-5	18	– 32	256 + 2K	68	12 / 10	4	17 / 4	USART + UART	–	21		8				P-LCC-84 P-MQFP-100	P-MQFP-100 for ROMless Version Only

* in preparation [1] CPU Clock

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