

# ***XC16Board***

Board REV. 200

## **Hardware Manual**

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## Introduction

This manual describes the functions of the XC16x Board that has been designed to evaluate the new Infineon XC161 and XC164 microcontrollers.

The XC16 board is an euro-sized (160 x 100mm) Board equipped with all necessary hardware such as non-volatile memory, SRAM memory, crystal oscillator (for clock generation), power supply and drivers for the interfaces.

## Features of the XC16 Board

- Infineon XC161CJ/XC164CS Controller in TQFP144/TQFP100-Package
- Two separate memory blocks - each equipped with 512KB Flash and 1MB SRAM (both expandable) for multiplexed and demultiplexed bus modes
- Onboard power supply which generates dual voltage for the XC16x
- Socket for crystal/oscillator (by default equipped with 8 MHz oscillator)
- Drivers for CAN, ASC(RS232), JTAG, OCDS-Interface and J1850 (XC161 only)
- 512 Bytes serial E<sup>2</sup>PROM

## Connectors

The XC16x Board offers a wide variety of connectors:

- SUB-D9 connector for ASC0 Interface via RS 232 port
- 10pin header (2x5) for ASC1 Interface (second RS 232 port)
- Sub-D25 connector (on-board wiggler) and 16-pin header for JTAG interface
- 10pin header (2x5) for J1850 Interface (XC161 only)
- Two 10pin (2x5) Headers connected to the TwinCAN Module
- Eight additional connectors (bus expansion, ADC/GPIO, peripherals and CAPCOM unit)

## Components

- LEDs to validate power supply (dual voltage)
- LED indicating /RSTIN active state
- LED showing /RSTOUT active state
- General purpose LED
- Reset switch
- NMI switch

## Jumpers

- Two jumpers to deselect on-board RS232 transceiver for communication via ASC0 and ASC1 (both can be disconnected separately)
- Onboard wiggler (OCDS Interface) can be disabled

## DIP Switches

The XC16x Board has 5 different DIP selection fields.

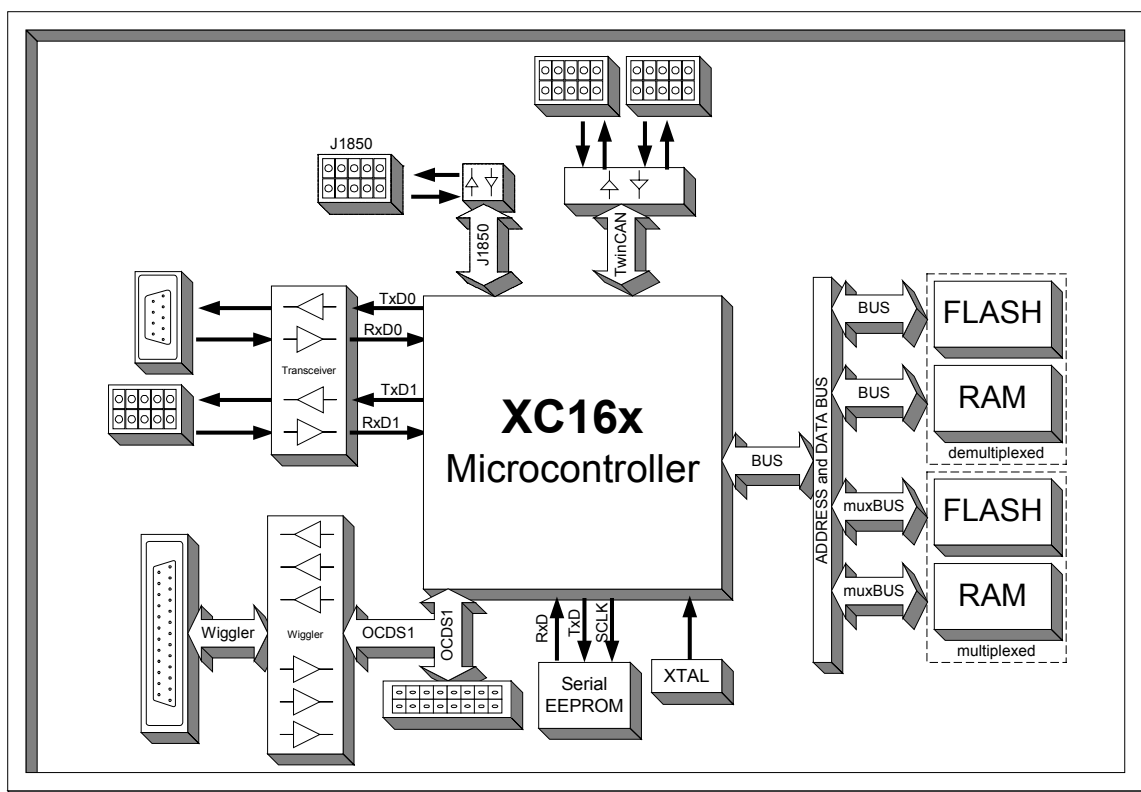
1.	S102 and S103	PORT0 configuration
2.	S106	Startup configuration
3.	S104 and S105	/CS assignment
4.	S101	/CS configuration
5.	S401	Peripheral control

### DIP Selection Fields

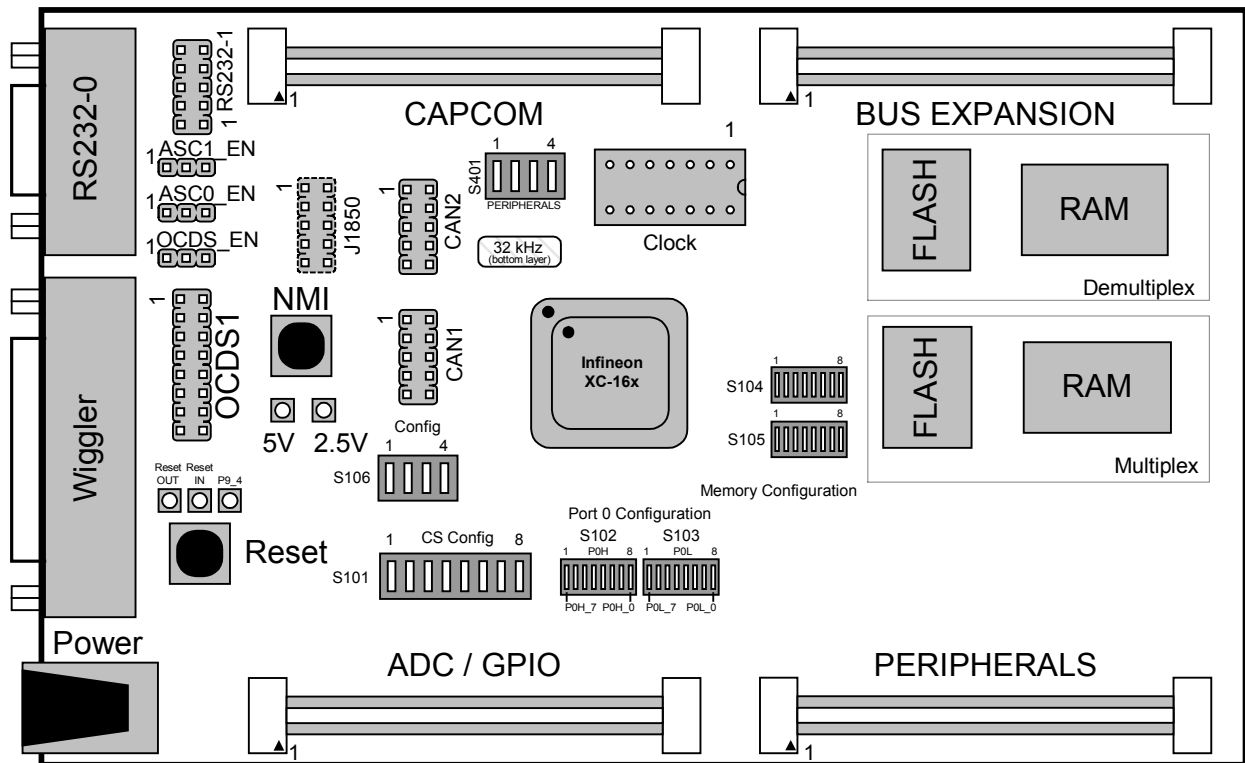
With these switches you can select MCU and peripheral configuration, for example:

- Startup system configuration can be determined by selecting levels of PORT\_0 and special pins
- Function of /RSTOUT behavior
- Startup mode (internal or external start, Bootstrap Loader mode etc.)
- External bus type (8 and 16 Bit, multiplexed and demultiplexed)
- Behavior of /WR signal
- Number of /CS-Lines
- Number of segment address lines
- Input frequency range (oscillator and crystal range)
- Function of PLL/ OWD can be turned on/off
- Connection of /CS0 and /CS1 to external FLASH and SRAM

## Architectural Overview



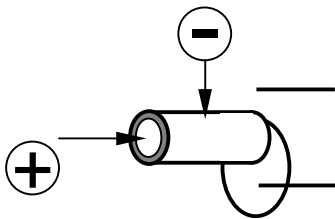
## Layout Overview



*Note: Dashed parts are not available on Boards with XC164 MCU*

## Power Supply

The XC16x Board needs an external power supply. A regulated DC power supply from 9 to 12 Volts can be connected to the power connector.



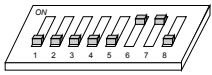
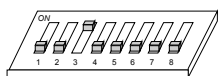
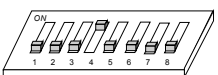

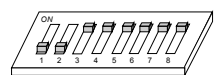
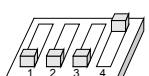
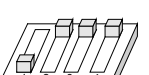
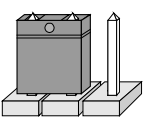
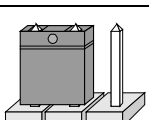
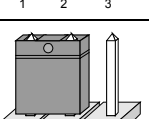
*Ensure correct polarity!*

## Default Configuration

By default, the XC16x Board is configured as follows:

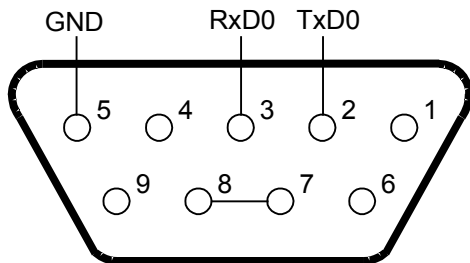
- Program execution starts at vector 0x0000 in external SRAM
- XC16x uses 16 bit demultiplexed bus and 2 segment address lines – therefore up to 256KB external memory can be addressed
- Bootstrap loader enabled
- CS0 is connected to SRAM, CS1 is connected to Flash
- Oscillator range is configured to “010” (8 - 12 MHz crystal range)
- CPU works @ 20 MHz
- Pin /EA tied to ground (program execution out of external memory)
- Peripheral Control Switches S401.1, S401.2 and S401.3 are turned on

## Description of Jumpers and Switches

Name in schematic	Default configuration	Description
S101		CS assignment  <i>(Default: /CS0 is connected to SRAM and /CS1 is connected to FLASH)</i>
S102		Port 0 (higher byte) configuration Position "OFF" means pin is open and due to internal pull-up resistors "high"  <i>(Default: input frequency range 6 – 8.3 MHz)</i>
S103		Port 0 (lower byte) configuration Position "OFF" means pin is open and due to internal pull-up resistors "high".  <i>(Default: Bootstrap Loader Mode 0 activated)</i>
S104		Disconnects A16...A23 from port 4 (Position "ON" means XC161-Pins and RAM/FLASH address lines are connected)  <i>(Default: only A16 and A17 are connected to ext. Memory)</i>
S105		Connects unused address lines of FLASH/RAM to GND (Position "ON" means address line is connected to GND)  <i>(Default: Unavailable address lines (A18..A23) connected to ground)</i>
S106		Startup configuration on pins /RD, /WR, ALE, /EA  <i>(Default: external access is enabled)</i>
S401		Enable/disable CAN1/CAN2 transceiver Enable/disable J1850 transceiver (XC161 only)  <i>(Default: CAN1, CAN2, J1850 Transceivers are enabled)</i>
JP401 ASC0_EN		1-2 Assign ASC0 to the RS232 transceiver (available on DB9)  <i>(Default: ASC0 is available on RS232 interface)</i>
JP402 ASC1_EN		1-2 Assign ASC1 to the RS232 transceiver (available on DB9)  <i>(Default: ASC1 is available on 2x5 header)</i>
JP501 OCDS_EN		1-2 Enable / disable onboard wiggler  <i>(Default: Onboard wiggler enabled)</i>

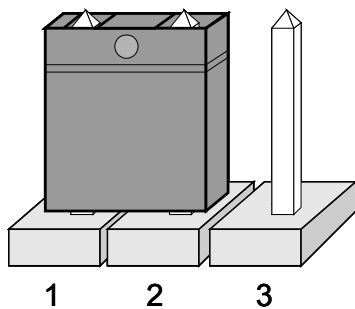
## Headers and Connectors

### RS-232 Connector (P401) – ASC 0

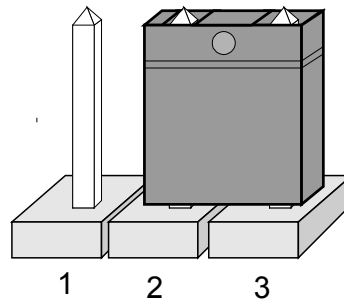


### Jumper JP401

The onboard RS-232 interface (DB9) is assigned to the ASC0 interface of the controller. For same reason the ASC0 can be disconnected from the transceiver.

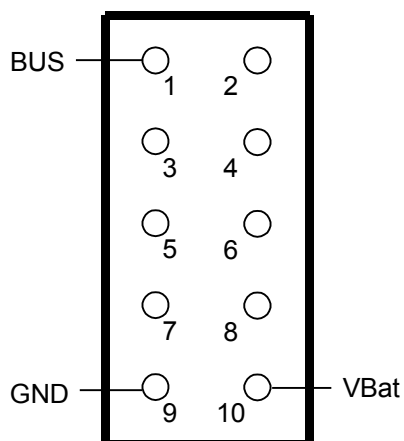


**JP401:** 1-2 : RS-232 connected to ASC0



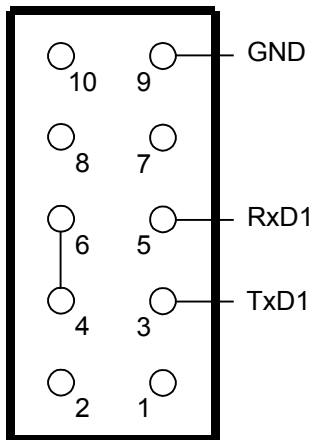
2-3 : RS-232 disconnected from ASC0

### J1850 Header (X402) (XC161 only)



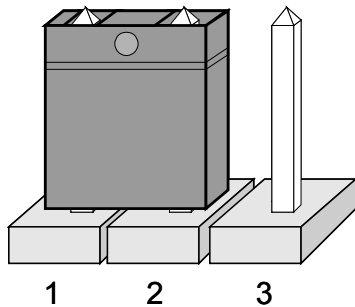


## ASC1 Header (X401)

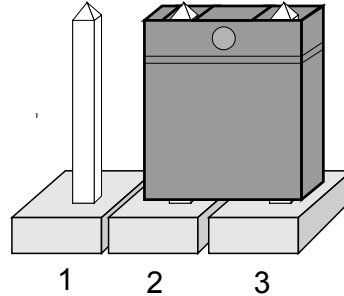


## Jumper JP402

The onboard RS-232 interface (2x5 header) is assigned to the ASC1 interface of the controller. For same reason the ASC1 can be disconnected from the transceiver.

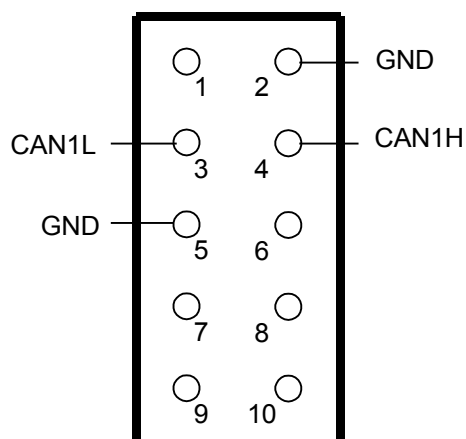


JP402: 1-2 : RS-232 connected to ASC1

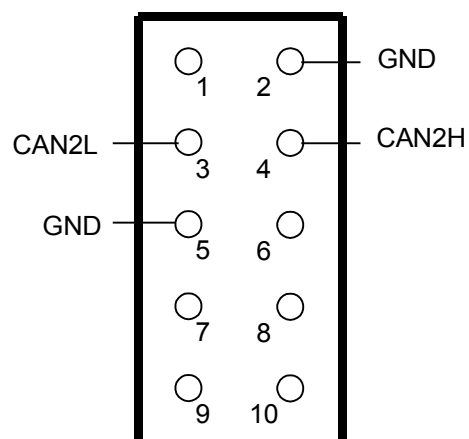


2-3 : RS-232 disconnected from ASC1

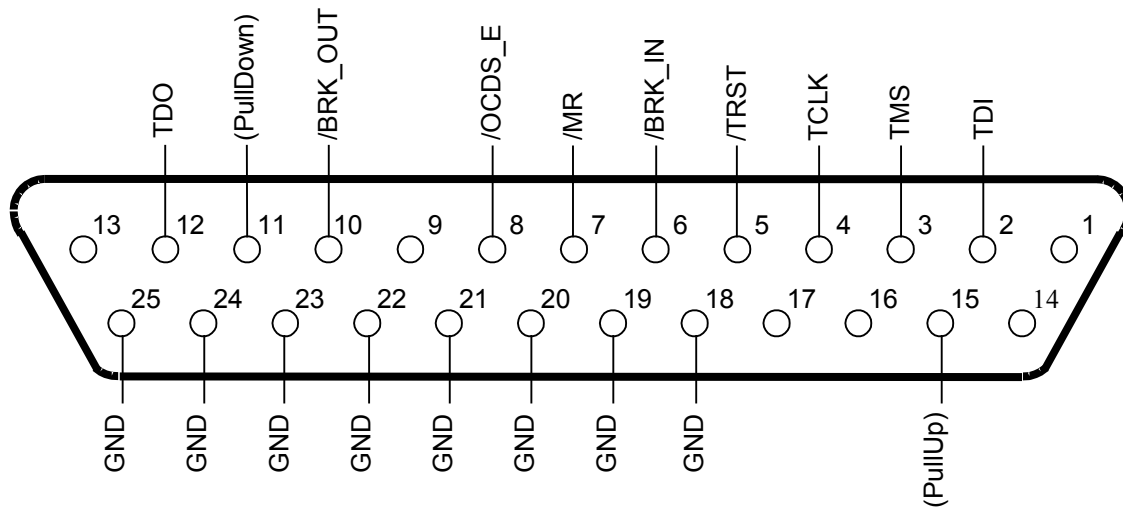
## CAN1 Header (X403)



## CAN2 Header (X404)

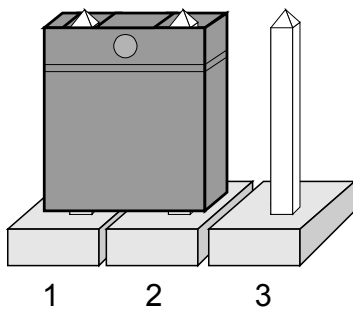


## OCDS Interface (On-board wiggler P501)

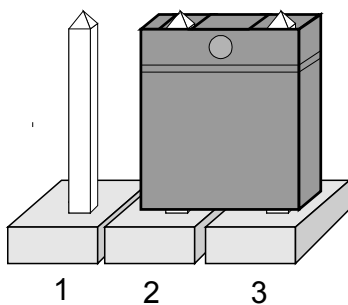


### Jumper JP501 (OCSD\_EN)

The onboard Wiggler can be enabled or disabled.

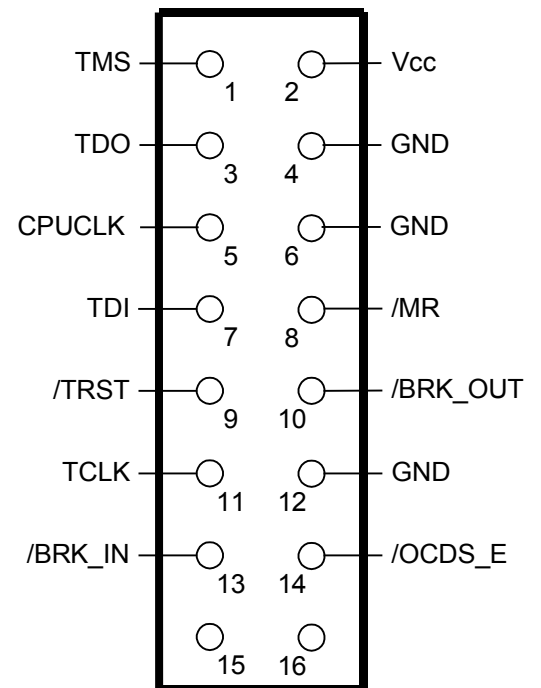


JP 501 1-2: Wiggler enabled



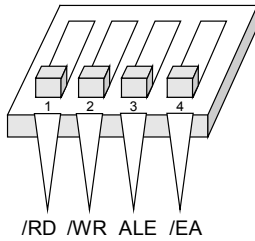
JP 501 2-3: Wiggler disabled

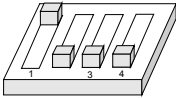
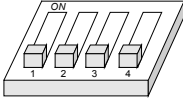

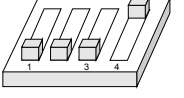
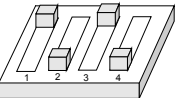
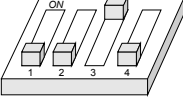
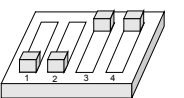
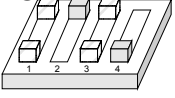
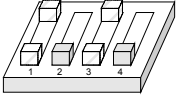
### onboard header X501



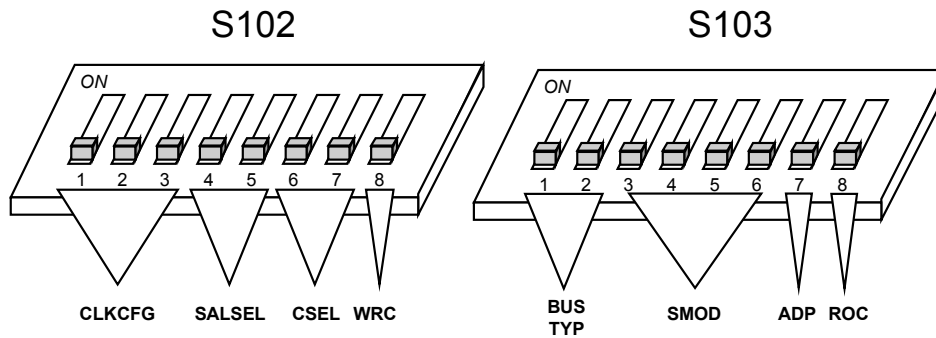
## Jumper Configurations



### Dip Switch S106





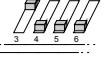
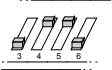
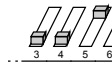
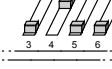
	/EA='1'		/EA='0'	
	RD='0'	RD='1'	/RD='0'	/RD='1'
<b>ALE='0'</b>	<b>Standard Boot</b> (bootstrap loader) 	<b>Standard internal</b> start 	<b>Standard external</b> start <b>PLL/OWD</b> switched <b>off</b> 	<b>Standard external</b> start <b>PLL/OWD</b> switched <b>on</b> 
<b>ALE='1'</b>	<b>Alternate boot</b> (bootstrap loader) 	<b>Alternate start</b> 	(do not use this configuration)	<b>Alternate start</b> <b>external</b> 
<b>/WR='0'</b>	RORMV = '1' (PIN 20.12 can be used as a general purpose IO) 		RORMV = '0' (/WR is "don't care")	
<b>/WR='1'</b>	RORMV = '0' 			

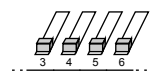
## Dip Switches S102 and S103









<b>S103: ROC (/RSTOUT Control)</b>	
<b>ON</b> 	/RSTOUT is deactivated at the end of reset
<b>OFF</b> 	/RSTOUT remains LOW until deactivation via user software





<b>S103: ADP (Adapter Mode selection)</b>	
<b>ON</b> 	Adapter mode – Device floats all pins
<b>OFF</b> 	Standard operation



<b>S103: SMOD (Startup Mode)</b>	
<b>ON-OFF-OFF-OFF</b> 	Alternate start (reset vector $\neq$ 0x0000)
<b>OFF-ON-ON-OFF</b> 	Activate Bootstrap Loader Mode 1
<b>OFF-OFF- ON-ON</b> 	Startup configuration taken from on-chip memory
<b>OFF-OFF-ON-OFF</b> 	Activate Bootstrap Loader Mode 0

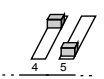
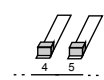
OFF-OFF-OFF-OFF 	Standard start
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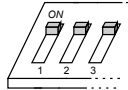
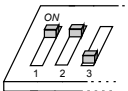
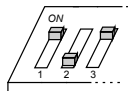
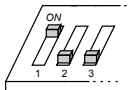
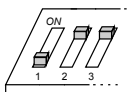
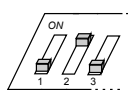
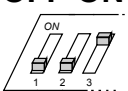
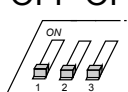
<b>S103: BUSTYP Bus Type</b>	
ON-ON 	8 bit data bus, demultiplexed
ON-OFF 	8 bit data bus, multiplexed
OFF-ON 	16 bit data bus, demultiplexed
OFF-OFF 	16 bit data bus, multiplexed

<b>S102: WRC (Write Configuration)</b>	
ON 	Pins /WR and /BHE act as /WRL and /WRH
OFF 	Pins /WR and /BHE act /WR and /BHE

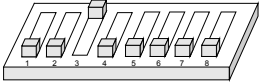
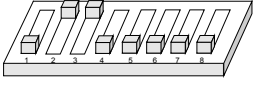
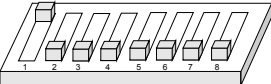
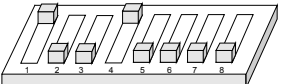
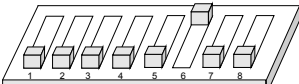
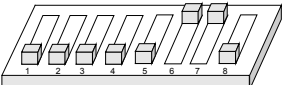
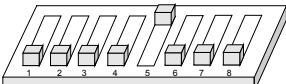
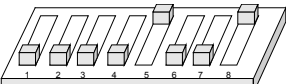
<b>S102: CSSEL Number of Chip select lines</b>	
ON-ON 	3 /CS lines
OFF-ON 	No /CS lines
ON-OFF 	2 /CS lines
OFF-OFF 	5 /CS lines

<b>S102: SALSEL Segment Address Line Select</b>	
ON-ON 	4-bit segment address lines (A19...A16)
OFF-ON 	8-bit segment address lines (A23...A16)

ON-OFF 	No segment address lines
OFF-OFF 	2-bit segment address lines (A17...A16)


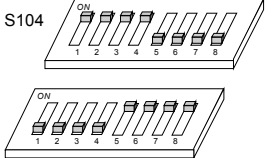

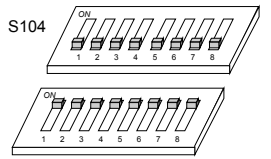

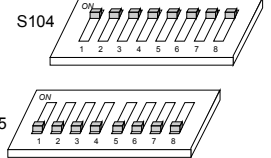

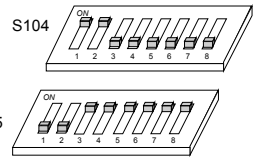
<b>S102: CLKCFG Clock Generation Mode Configuration</b>		
ON-ON-ON 	$f_{IN} = 8 - 50 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 0,5$
ON-ON-OFF 	$f_{IN} = 12 - 16 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 2,5$
ON-OFF-ON 	$f_{IN} = 8 - 12 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 2,5$
ON-OFF-OFF 	$f_{IN} = 4 - 40 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 1$
OFF-ON-ON 	$f_{IN} = 4 - 6 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 5$
OFF-ON-OFF 	$f_{IN} = 12.5 - 16 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 2$
OFF-OFF-ON 	$f_{IN} = 6 - 8.3 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 4,5$
OFF-OFF-OFF 	$f_{IN} = 8.3 - 12.5 \text{ MHz}$	$f_{PLL} = f_{OSC} \times 3$

## Dip Switch S101

<b>S101: External Memory Configuration</b>		
<b>1-4</b>	<b>4-8</b>	<b>Demultiplexed bus mode</b>
OFF-OFF-ON-OFF	OFF-OFF-OFF-OFF	/CS0 connected to ext. RAM (no Flash)
		
OFF-ON-ON-OFF	OFF-OFF-OFF-OFF	/CS0 connected to ext. RAM, /CS1 connected to ext. Flash
		
ON-OFF-OFF-OFF	OFF-OFF-OFF-OFF	/CS0 connected to ext. Flash (no RAM)
		
ON-OFF-OFF-ON	OFF-OFF-OFF-OFF	/CS0 connected to ext. Flash, /CS1 connected to ext. RAM
		
<b>1-4</b>	<b>4-8</b>	<b>Multiplexed bus mode</b>
OFF-OFF-OFF-OFF	OFF-ON-OFF-OFF	/CS1 connected to ext. FLASH (no RAM)
		
OFF-OFF-OFF-OFF	OFF-ON-ON-OFF	/CS0 connected to ext. RAM, /CS1 connected to ext. FLASH
		
OFF-OFF-OFF-OFF	ON-OFF-OFF-OFF	/CS0 connected to ext. FLASH (no RAM)
		
OFF-OFF-OFF-OFF	ON-OFF-OFF-ON	/CS0 connected to ext. Flash, /CS1 connected to ext. RAM
		

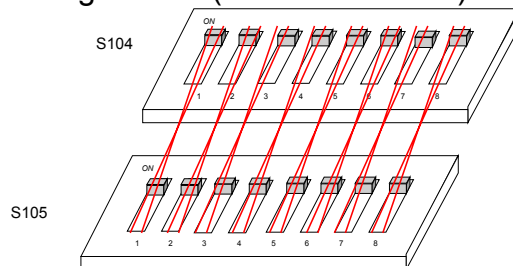
## Address Line Configuration

The XC61x board features all segmentation modes of the XC16x controller. In order to support less than 8 Bit segment address lines, all address lines from A16 to A23 can be tied to ground thus ensuring proper operation of the FLASH/ SRAM while freeing port 4 I/O lines.

Configuration according to SALSEL register		DIP switch configuration	
		S104	S105
<b>S103</b>			
ON-ON 	4-bit segment address lines	11110000	00001111 
ON-OFF 	no segment address lines	00000000	11111111 
OFF-ON 	8-bit segment address lines	11111111	00000000 
OFF-OFF 	2-bit segment address lines	11000000	00111111 

### Note:

Do **not** use the following configuration: (S104 AND S105)  $\neq$  0.





## DIP Switch S401 Peripheral Configuration

