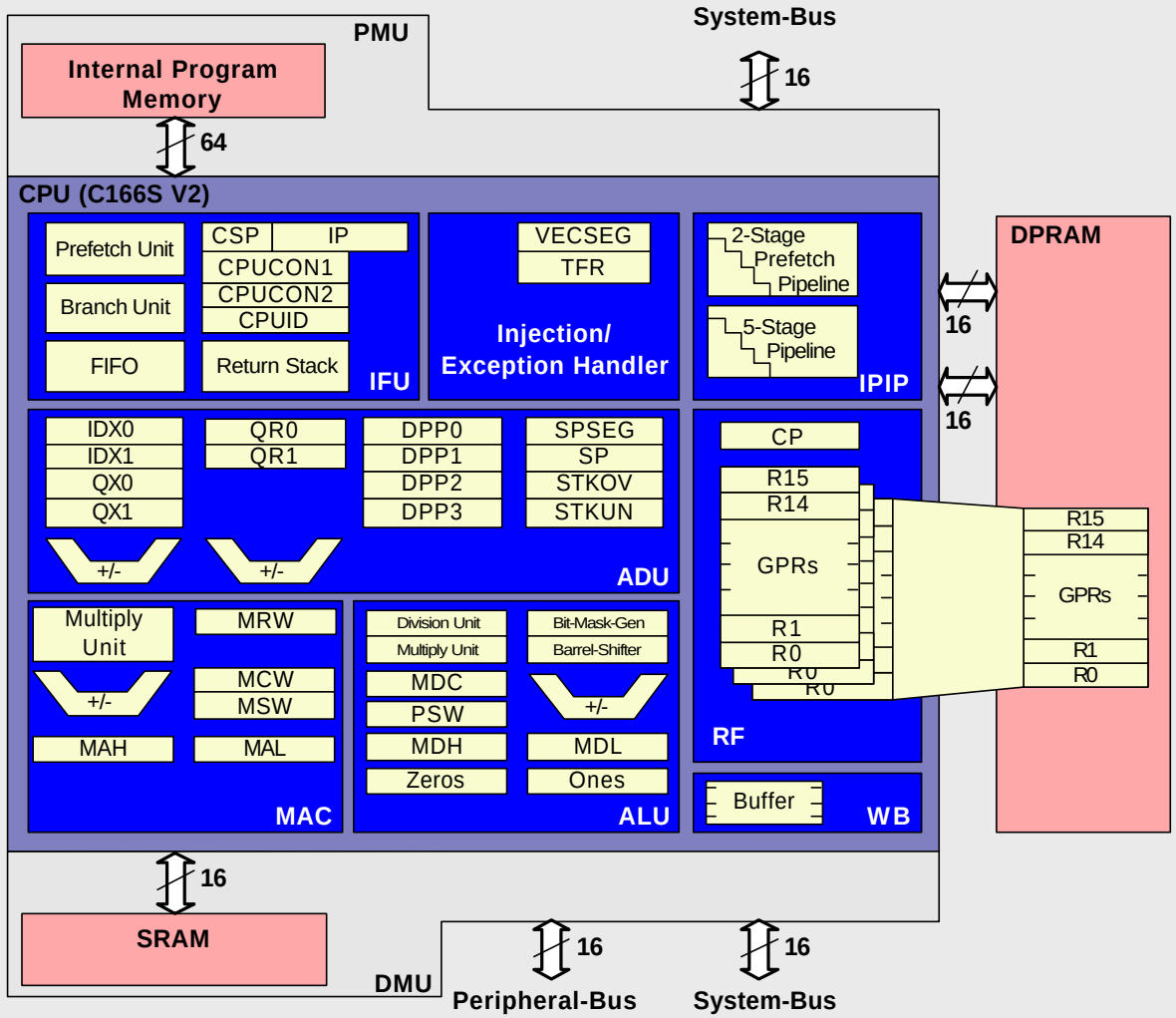
C166S-V2 CPU Architecture Block Diagram



C166S-V2 CPU Architecture
CPU main units (1)

- **I**nstruction **F**etch **U**nit (**IFU**)
  - High Bandwith Fetch Interface
  - Instruction FIFO
  - High Performance Branch-, Call, and Loop-Processing with instruction flow prediction
  - Return Stack
- Injection/Exception Handler
  - Handling of Interrupt Requests
  - Handling of Hardware Failures
- **I**nstruction **Pip**eline (**IPIP**)
  - 2-stage Prefetch Pipeline
  - 5-stage Execution Pipeline

C166S-V2 CPU Architecture
CPU main units (2)

- **A**ddress and **D**ata **U**nit (**ADU**)
  - 16-bit arithmetic unit for address generation
  - DSP address unit with a set of dedicated address- and offset pointers
- **A**rithmetic and **L**ogic **U**nit (**ALU**)
  - 8-bit and 16-bit Arithmetic Unit
  - 16-bit Barrel Shifter
  - Multiplication and Division Unit
  - Bit manipulation Unit
- **M**ultiply and **Ac**cumulate Unit (**MAC**)
  - 16-bit multiplier with 32-bit result generation
  - 40-bit Accumulator with 40-bit Barrel Shifter
  - Repeat Control Unit

C166S-V2 CPU Architecture
CPU main units (3)

- **R**egister **F**ile (**RF**)
  - One global register bank
  - Two local register banks
- **W**rite Back **B**uffer (**WB**)
  - 3-entries buffer
- **P**rogram **M**anagement **U**nit (**PMU**)
  - access internal program memory block (IMB)
  - 64 bit wide interface between CPU and internal program memory
  - control instruction fetch from external memory via EBC
- **D**ata **M**anagement **U**nit (**DMU**)
  - controls 16bit data flow in the system

C166S-V2 CPU Architecture
Instruction Set (1)

- Data manipulation
  - Arithmetic and boolean instruction
  - Multiple (up to 15) bit shift and rotate in only cycle
  - Bit to bit manipulation in internal RAM and SFR's
- Data movement
  - MOV instructions with all important addressing modes
  - Byte to word conversion
  - System stack (PUSH, POP) with over- and underflow control
  - User stack (MOV with auto increment and decrement)

C166S-V2 CPU Architecture
Instruction Set (2)

- Program manipulation
  - Jumps and calls / conditional jumps under 22 different conditions
  - Software- and hardware-Traps
  - Fast context switching
- DSP instruction set
  - 32-bit additions and subtraction
  - shift operations
  - 16-bit x 16-bit multiplication
  - multiplication with cumultative subtraction/addition

C166S-V2 CPU Architecture
Instruction Set (2)

- Special instructions for
  - Power consumption reduction and system Control
  - Non-interruptable instruction sequences
  - Extended addressing access

C166S-V2 CPU Architecture
Instruction fetch pipeline

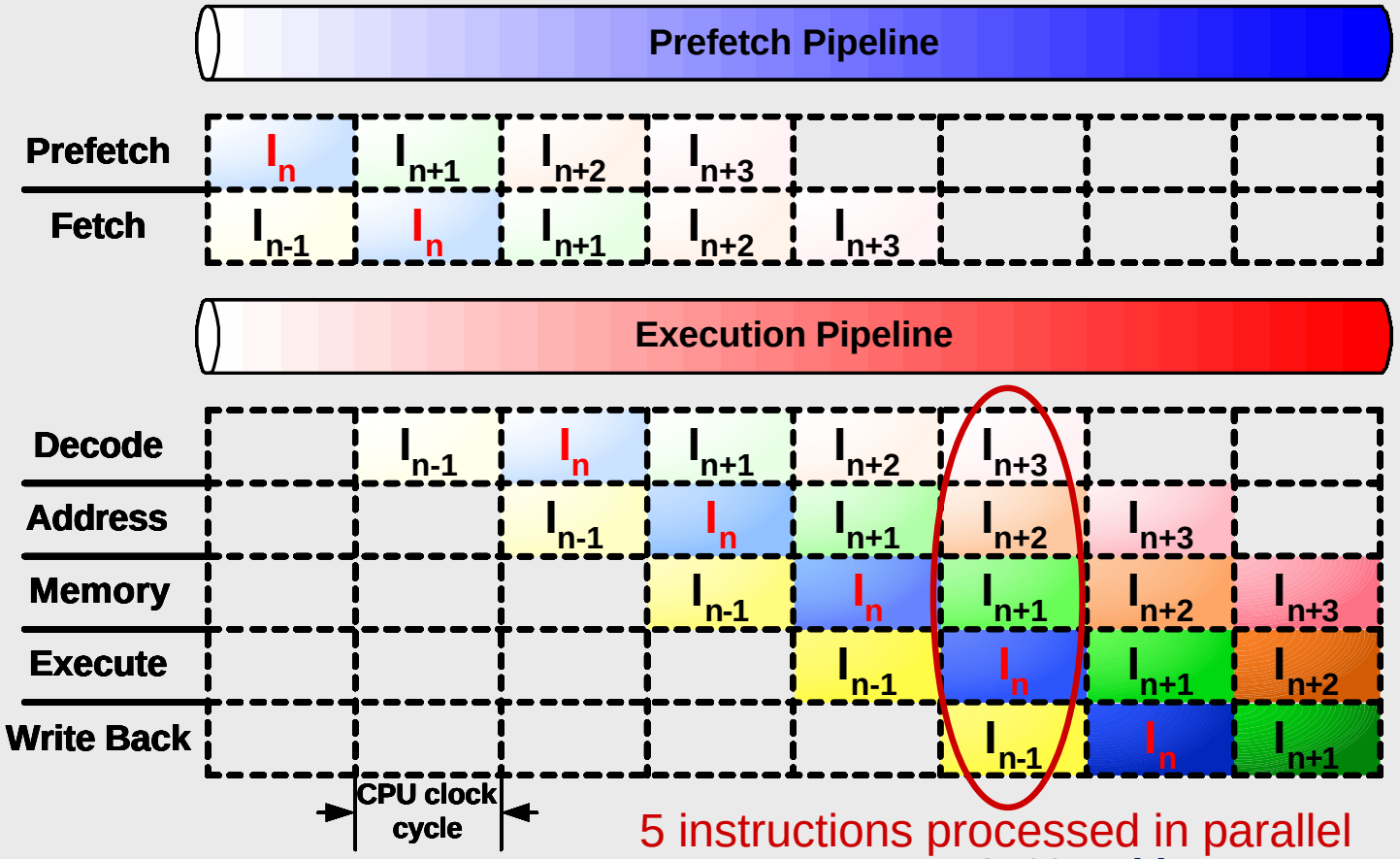
- 2-state instruction fetch pipeline
  - Pre-fetch
    - pre-fetch next instruction, decode branches, and predict if taken or not
  - Fetch
    - Fetch instruction predicted from branch prediction.

C166S-V2 CPU Architecture
Execution pipeline

- 5-stage execution pipeline
  - Decode
    - Instruction is decoded, and GPR read if indirect addressing is required
  - Address
    - Operand addresses are calculated. SP is modified if implicit stack operation is required
  - Memory
    - Operand values are fetched
  - Execute
    - ALU or MAC operation performed, and condition flags updated. Explicit SFR writes performed, indirect auto GPR pointers modified
  - Write Back
    - IRAM data written back, SRAM data written to write back buffer

C166S-V2 CPU Architecture
Pipeline

- 2-stage prefetch pipeline
- 5-stage execution pipeline



C166S-V2 CPU Architecture
General Purpose Register (GPR)

- Up to 16 GPRs = 1 Register bank
  Consisting of max.
  - 8 Word-Registers
  - 8 Word-Registers with lower and higher Byte access
- The GPRs are bit-addressable
- Any Register bank can be freely allocated in internal DPRAM
- The location of the active Register bank is determined by Context Pointer (CP)
- CP can be easily switched, to select another Register bank
  e.g. SCXT CP, #New_Regbank

C166S-V2 CPU Architecture
General Purpose Register (GPR)

- C166S-V2.0 has a set of 3 Register Files:
  - several memory mapped banks of GPRs which are located in the internal DPRAM (equal to C166) (global register bank - Bank0)
  - two special non memory mapped GPRs (local register bank - Bank1 and Bank2)
  - The different banks are selected by two bank select bits inside the PSW
  - The local not memory mapped banks can be used for fast context switching
  - GPRs located in the DPRAM

C166S-V2 CPU Architecture
General Purpose Register (GPR)