C166S-V2 CPU Architecture
Additional features to C16x

XC16x

- C166S-V2 CPU
  - VHDL synthesised core
  - 2 stage prefetch pipeline
  - 5 stage interlocked pipeline
  - Single cycle CPU
  - 50ns instruction @20MHz
  - Multiplication (16-bit x 16-bit) in 1 CPU cycle, (50ns @20 MHz)
  - Division (32-bit / 16-bit) in 21 CPU cycles, (1.05µs @20MHz)

C16x

- C166 CPU
  - Full custom layout
  - 4 stage pipeline
  - Double cycle CPU
  - 100ns instruction @20MHz
  - Multiplication (16-bit x 16-bit) in 5 CPU cycle, (500ns @20 MHz)
  - Division (32-bit / 16-bit) in 16 CPU cycles, (1.6µs @ 20 MHz)

C166S-V2 CPU Architecture
Additional features to C16x

XC16x

- C166S-V2 CPU
  - High Performance Branch-, Call, and Loop-Processing with instruction flow prediction
  - Zero cycle jump execution
  - Improved BFLD instruction (BFLDH bitoff,#mask8,#data8) bits to be modified must be indicated by a ’1’ within the mask
- MAC unit

C16x

- C166 CPU
  - Limited Loop Processing
  - BFLD instruction