C166S-V2 CPU Architecture Overview (1)

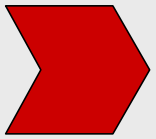
- High Performance 16-bit CPU
  - Op-code fully upward compatible with C166 family
  - 5-stage execution pipeline
  - 2-stage instruction fetch pipeline
  - Single clock cycle instruction execution
  - 25 ns instruction time @ 40 MHz CPU clock
  - 40 MIPS @ 40 MHz CPU clock
  - Pipeline with forwarding that controls data dependencies in hardware
  - Multiple high bandwith internal busses for code and data

C166S-V2 CPU Architecture Overview (2)

- High Performance 16-bit CPU
  - Fast multiplication (16 x 16 bit), (1 cycle, 25ns @ 40MHz)
  - Fast background division (32/16-bit), (up to 21 cycle, 525ns @ 40MHz)
  - High performance branch, call and loop processing
    - Branch detection and branch prediction (JMPA, CALLA..)
    - Zero cycle jump execution
  - Built-in advanced MAC unit
    - Single cycle multiply and accumulate instruction (MAC) execution (25ns @ 40MHz)
    - DSP instruction set (CoXXX arithmetic instructions)
  - Enhanced boolean bit manipulation facilities
  - Additional Instructions to support HLL and operating systems

C166S-V2 CPU Architecture Overview (3)

- High Performance 16-bit CPU
  - Register-based design with multiple variable register banks
  - 2 additional fast register banks
    - Single-cycle context switching support
  - 16 MByte total linear address space for code and data



Approximately 1.7 to 2.x times more performance than the C166 CPU