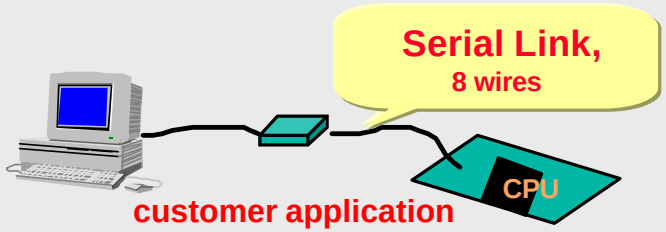
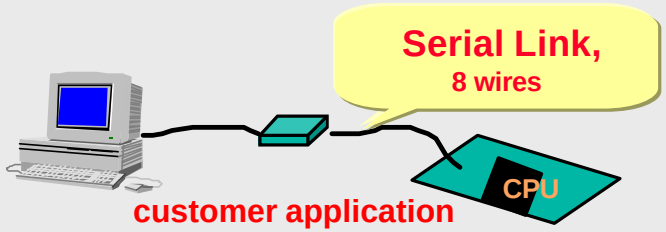
XC16x Emulation Concept
OCDS Level 1 (On Chip Debug Support)



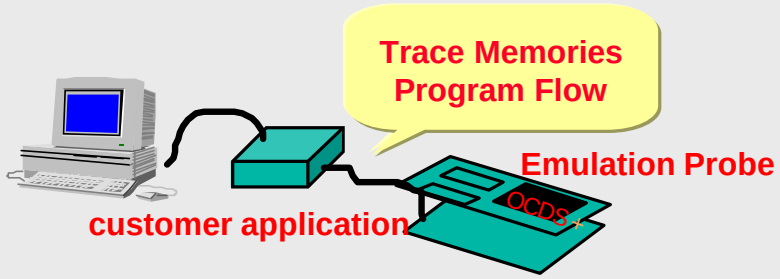
- OCDS Level1: On-Chip-Debug-Support
  - Low cost concept
  - Available on all production chip
  - Controlled via a JTAG link (8 wires)

XC16x Emulation Concept
OCDS Level 1 (On Chip Debug Support)



- Features
  - Run control
  - Program breakpoint / trigger also in internal FLASH
  - Read/Write on the fly
  - Flash Programming via JTAG
  - access to:
    - on chip memories
    - CPU core state
    - SFRs
    - Peripherals
    - memories/devices at the external bus interface

XC16x Emulation Concept
OCE (On Chip Emulation)



- OCE: On-Chip-Emulation
  - Enhanced concept
  - Available in a dedicated package
- aditional Features
  - Run control
  - complex Program / Data breakpoints
  - Program trace

XC16x Emulation Concept
OCE (On Chip Emulation)

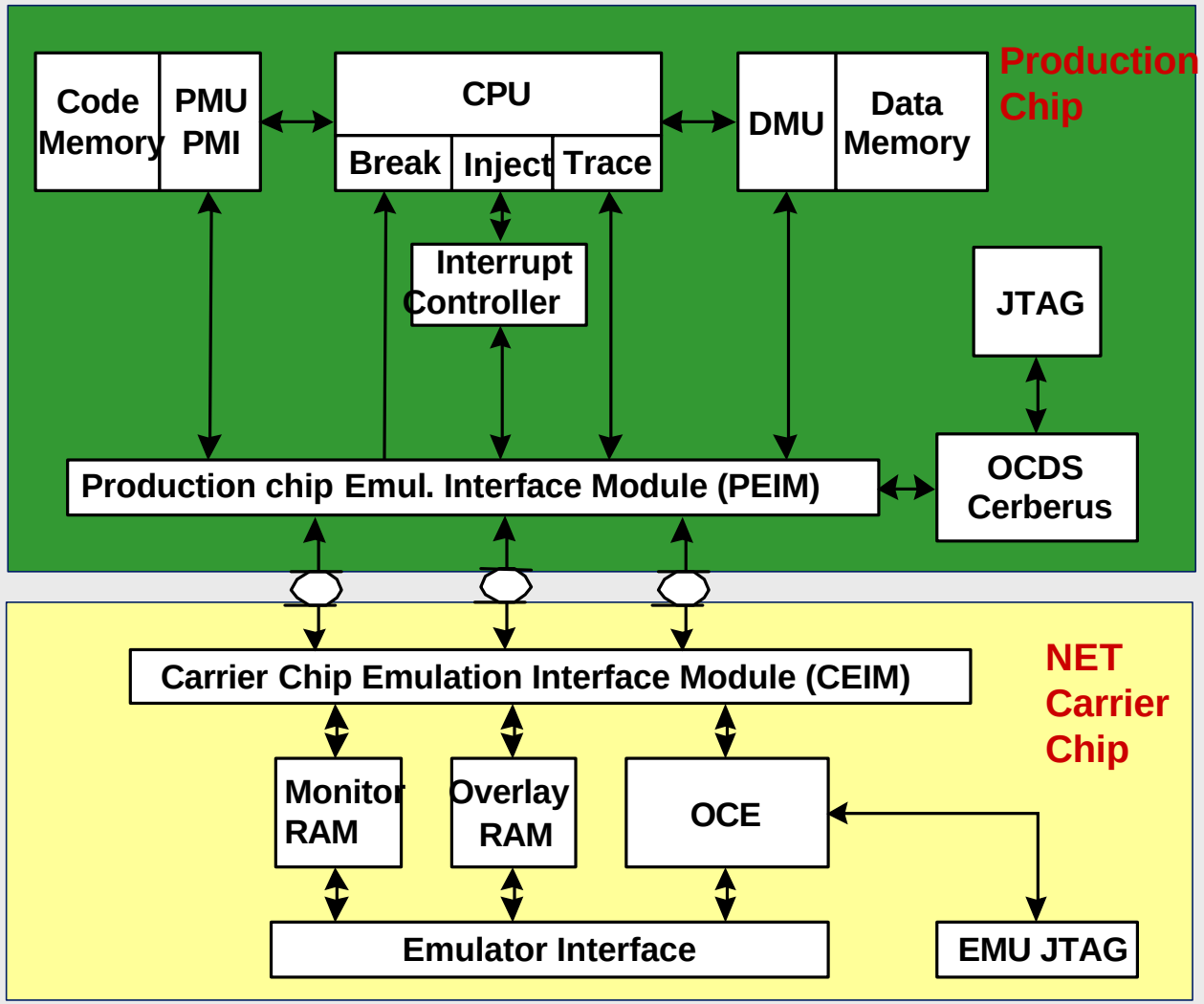
- New Emulation Technologies (NET)
  - production chip is connected to a NET carrier chip
  - emulation resources distributed on both chips:

- Production Chip:
  - OCDS and Cerberus for standard debugging
  - JTAG
  - program Flash memory
  - communication to carrier chip via PEIM (Production chip Emulation Interface Module)

- NET Carrier Chip:
  - OCE for high-end debugging
  - JTAG and emulator interface
  - Overlay RAM to emulate the FLASH memory (128 kBytes)
  - communication to production chip via CEIM (Carrier chip Emulation Interface Module)
  - monitor RAM (128 kBytes) for monitor code (can be locked)
  - trace port for internal signals

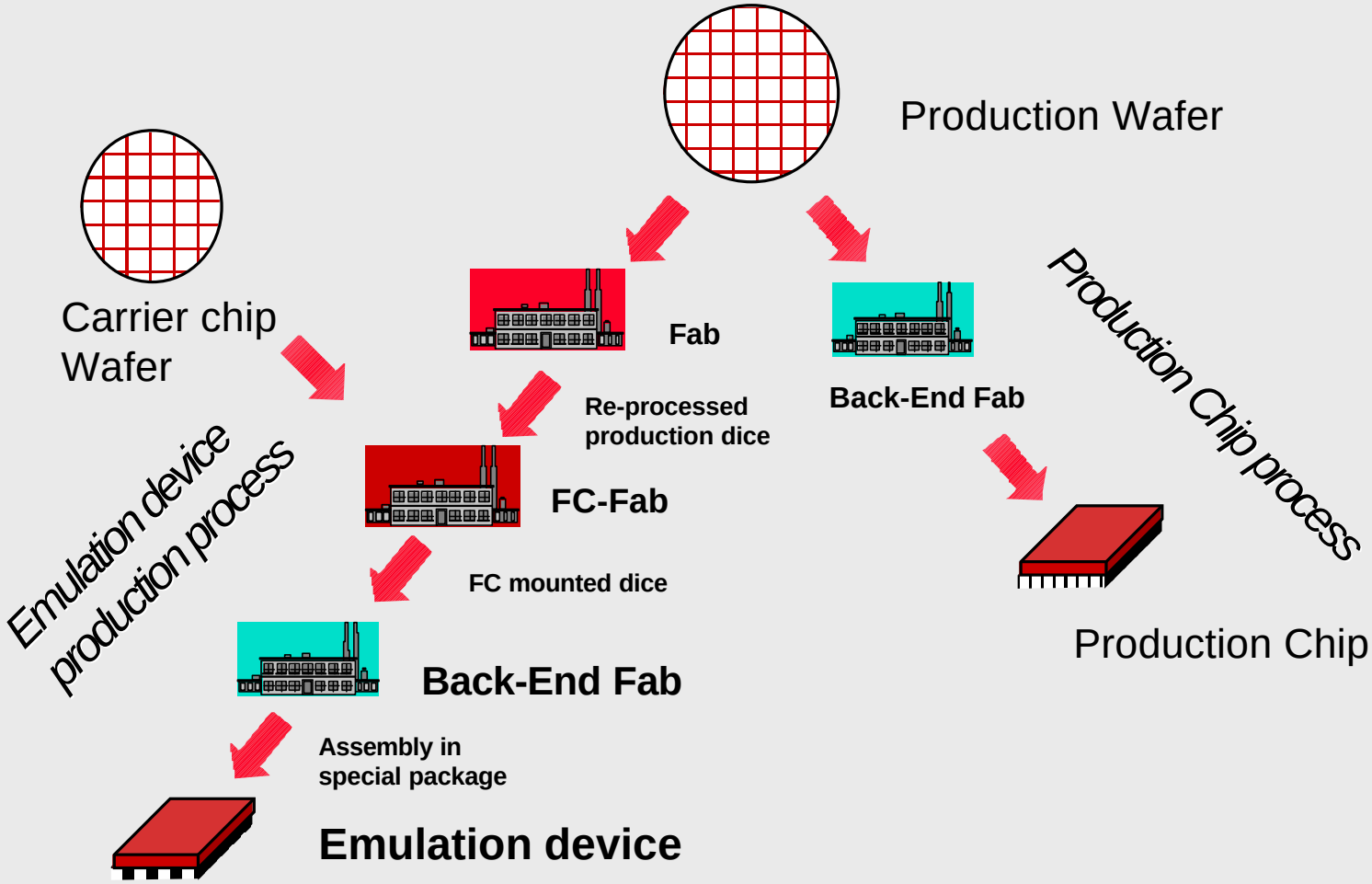
XC166 architecture

XC16x Emulation Concept
OCE (On Chip Emulation) - Block Diagram



XC166 architecture

XC16x Emulation Concept
Emulation Device Manufacturing



XC16x Emulation Concept
Emulation Device

XC161/XC164
Production chip flipped on the NET carrier chip for real time emulation support.

Advantage:
The emulation behaviour is equivalent to production chip.
This simplifies your debug effort

XC166 architecture

XC16x Emulation Concept
Emulation Memory

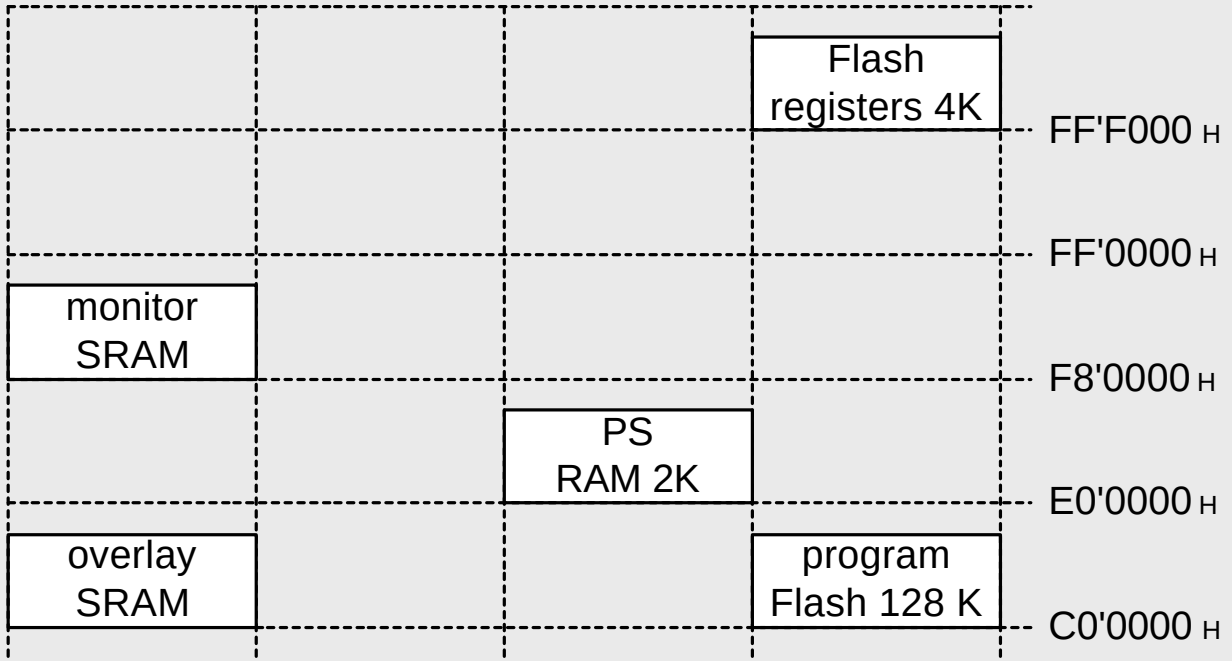
- Overlay Memory (128 kBytes on the carrier chip)
  - used to emulate the Flash memory
  - identical timing behavior compared to Flash access
  - can be loaded with code by emulator interface
  - SW can select whether the program is executed from the Flash or from the overlay memory (same address range)
- Monitor Memory (128 kBytes on the carrier chip)
  - used to store monitor or emulation routines or emulation data
  - can be protected (against user code access)
  - indication if the CPU accesses this memory area
- Status of Device
  - SW can check if an emulation device is connected

XC16x Emulation Concept
Emulation Concept

- XC166 Architecture Debugging Strategy
  - a breakpoint or another selected event occurs while the application SW is running
    - the instruction pipeline is stalled for application code fetch (break = no new instruction is executed)
    - instructions can be injected into the CPU, controlled by the debugger
    - the injected instruction can be a jump to a monitor routine in the monitor memory, that is then executed
    - after the monitor routine, the application code fetch can be enabled again
    - single step debugging also supported

XC16x Emulation Concept
Memory Overlay

- Program Memories (access via IMB, also for data):
  - Program Flash with parallel overlay SRAM for emulation
  - Program RAM (PSRAM)
  - Monitor SRAM for emulation



XC166 architecture