

C166S-V2 CPU Architecture Interrupt/PEC

Additional features to C16x

XC16x

- 16-Priority-level interrupt system
 - up to 128 sources with 16 levels on 8 groups
- PEC
 - Triggered by interrupts from level 15 to 8
 - 24 bit addressing
 - increment of source and / or destination pointers
 - Additional End of PEC interrupt node

C16x

- 16-Priority-level interrupt system
 - up to 64 sources with 16 levels on 4 groups
- PEC
 - Triggered by interrupts from level 15 to 14
 - 16 bit addressing
 - increment of source or destination pointers
 - End of PEC interrupt at regular PEC node

XC166 architecture

C166S-V2 CPU Architecture Interrupt/PEC

Additional features to C16x

XC16

- Context Switch
 - 19 cycle (950ns @20 MHz) context switch for Global Register Banks
 - 0 cycle context switch for 2 new register banks (not memory mapped)

C16

- Context Switch
 - 4 cycle (400ns @20 MHz) context switch for Global Register Banks