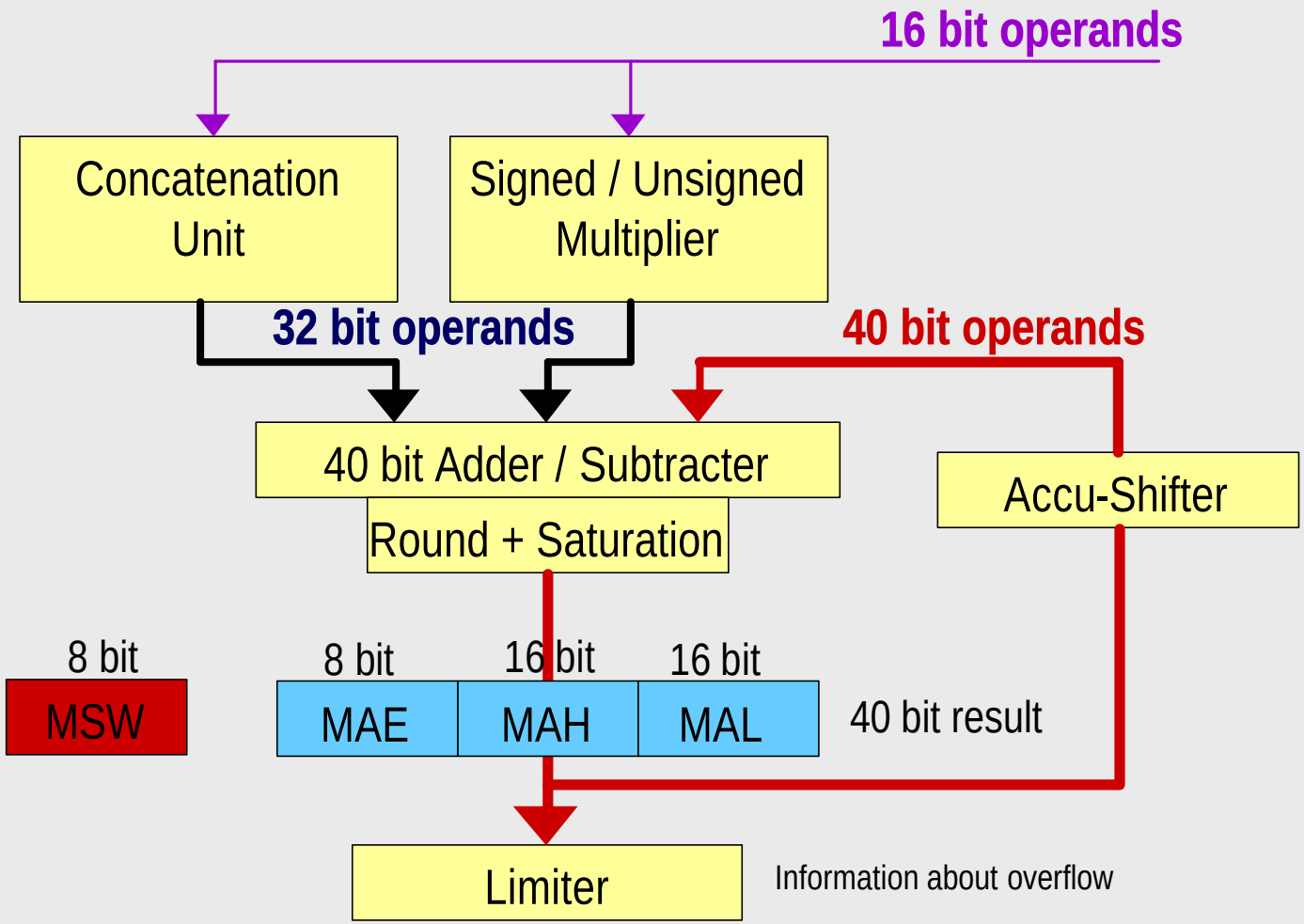
C166S-V2 CPU Architecture
Multiply Accumulate Unit (MAC)

- MAC Unit consists of
  - 16 bit by 16 bit signed / unsigned multiplier with signed result
  - Concatenation unit
  - Scaler (one bit left shifter) for fractional computing of signed data
  - 40bit Adder / Subtracter
  - 40bit Accumulator
  - Data limiter
  - Accumulator shifter
  - Repeat counter

C166S-V2 CPU Architecture
Multiply Accumulate Unit (MAC)



C166S-V2 CPU Architecture
Multiply Accumulate Unit (MAC)

- MAC Unit instruction set is derived from unused opcodes within the C166 machine opcodes, hence MAC does not get used if directly porting existing assembly code.
- MAC registers are:
  - IDX0, IDX1 — Operand address pointers (Fxxxh) (Can be auto incremented / decremented by 2 or by QX0, QX1)
  - QX0, QX1 — Offset registers for IDX0, IDX1
  - MCW — MAC unit control word
  - MSW — MAC unit status word
  - MAE — MAC unit extend (8 bits)
  - MAH — MAC unit high word
  - MAL — MAC unit low word
  - MRW — MAC unit loop repeat counter

C166S-V2 CPU Architecture
Multiply Accumulate Unit (MAC)

- Infineon will provide
  fast DSP libraries to utilise the MAC for:
  - common DSP filters
    - 16 & 32 bit FIR filter
    - IIR filter
    - 16 & 32 bit adaptive filter
  - matrix functions
    - matrix multiplication
  - arithmetic functions
    - complex addition, subtraction and multiplication
  - FFT
- Latest releases of compilers supports MAC assembly code generation by a command line switch. e.g. -EXTMAC