Internal Initialization Phase

- Reset Phases
  - 1.Phase) external reset phase
    - cover the time until /RSTIN = 1 (HW reset)
  - 1.Phase) ore pre-reset phase
    - Is triggered by SW reset
  - 2.Phase) internal reset phase
    - CPU reset, modules reset
    - duration of the internal reset phase can be configured (bitfield RSTLEN in register RSTCON)
  - 3.Phase) initialization phase
    - Startup code executed from the on-chip startup memory
    - User initialization code executed from user memory

Clock Generation Control

- The clock generation path is controlled via the PLL control register PLLCON
- The oscillator delivers the system´s clock signal
  - external crystal (optimized 4-16 MHz)
  - external clock signal up to 40 MHz
- Input clock divider adjust the system´s clock signal to the input freq. Range of the PLL (optimized 4 - 35 MHz)

Clock Generation Control

- The PLL multiplies the input frequency by a selectable factor
  - PLLMUL PLL multiplier factor (*8 to * 32)
  - The PLL can be bypassed
  - For device testing the complete clock generation can be bypassed by directly driving the system with the osc. Clock
  - Output clock divider scales the PLL´s output frequency
  - PLLODIV PLL output divider (1:1 to 1:16)

Register Security Mechanism

- Some registers which control critical functions and modes are protected after EINIT.
  - 3 Security levels with password protection
    - **Write Protect Mode** - all protected registers are read only
    - **Secured Mode** - protected registers can be written if preceded by a command sequence
    - **Unprotected Mode** - no protection, protected registers can be written

Power Management Control Block

- Power reduction mode
  - Idle Mode
    - All enabled peripherals are operating normally
    - CPU, PMU,DMU,EBC,Interr./PEC are stopped
    - Idle mode is terminated by interrupt requests, NMI
  - Sleep Mode
    - All internal clocking of blocks, including WDT is stopped
    - Sleep mode is terminated by an RTC or external interrupt,NMI
  - Power Down Mode
    - The CPU and all peripherals are stopped
    - Power down mode is terminated by a hardware reset

Watchdog Timer

- Watchdog Timer has been designed to recover software or hardware failure
- If the software fails to serve the Watchdog Timer a timer overflow generates a internal reset and pull the /RESETOUT pin low
- The watchdog timer is 16 bit wide and can be clocked with the peripheral clock either divided by 2, 4, 128, 256
- The upper 8 bits can be preset, the lower 8 bits are cleared upon each service access
- Compatible mode, DISWDT will only be executed before EINIT, SRVWDT
- Enhanced mode, watchdog timer can be disabled/enabled at any time

Watchdog Timer

Watchdog Timer Block Diagram