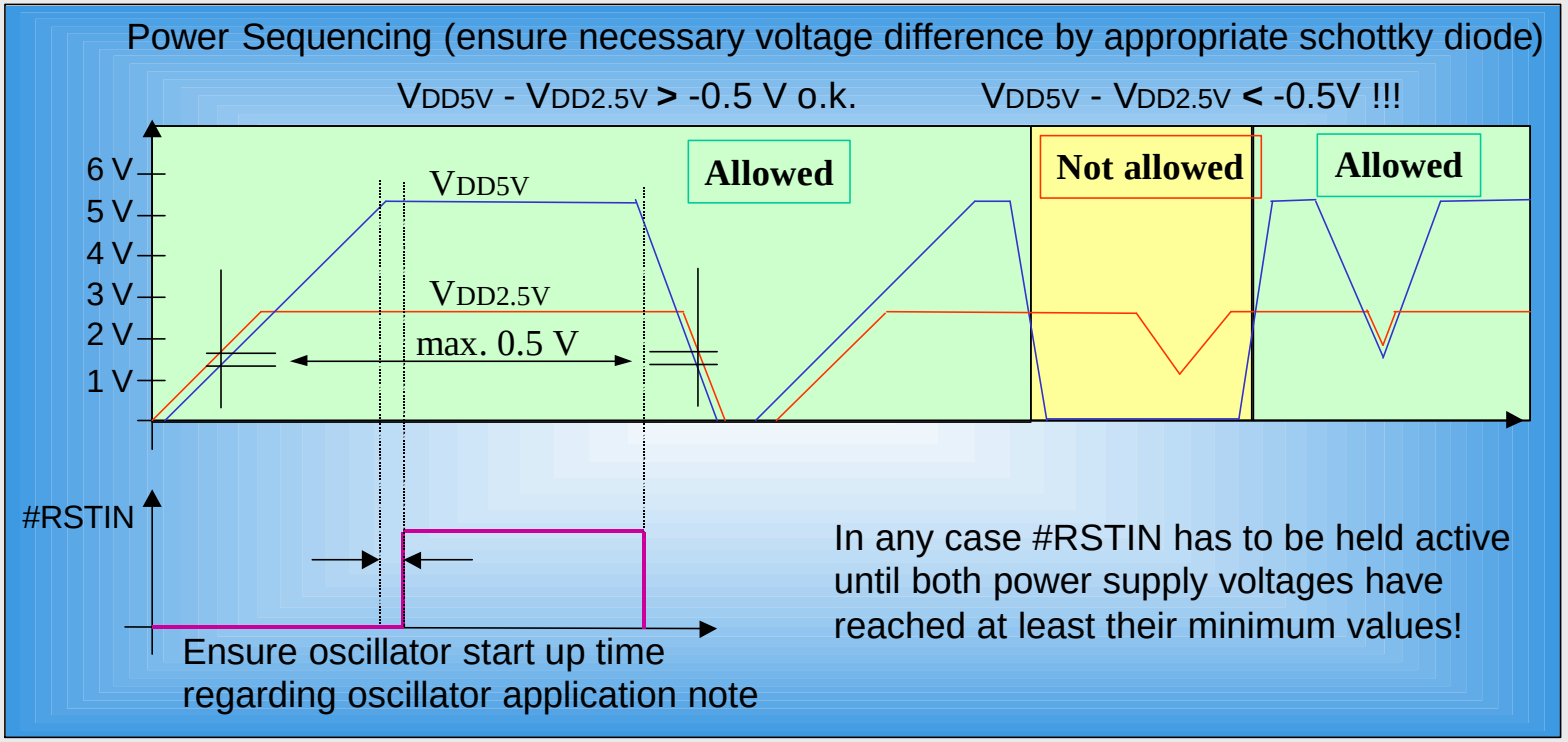
Power Supply

- Dual voltage power supply required.
  - 5V for I/O, ADC, and Port structures (Vddp)
  - 2.5V for internal core, and XTAL (Vddi)
  - It must be ensured that Vddp - Vddi is never less than -0.5V



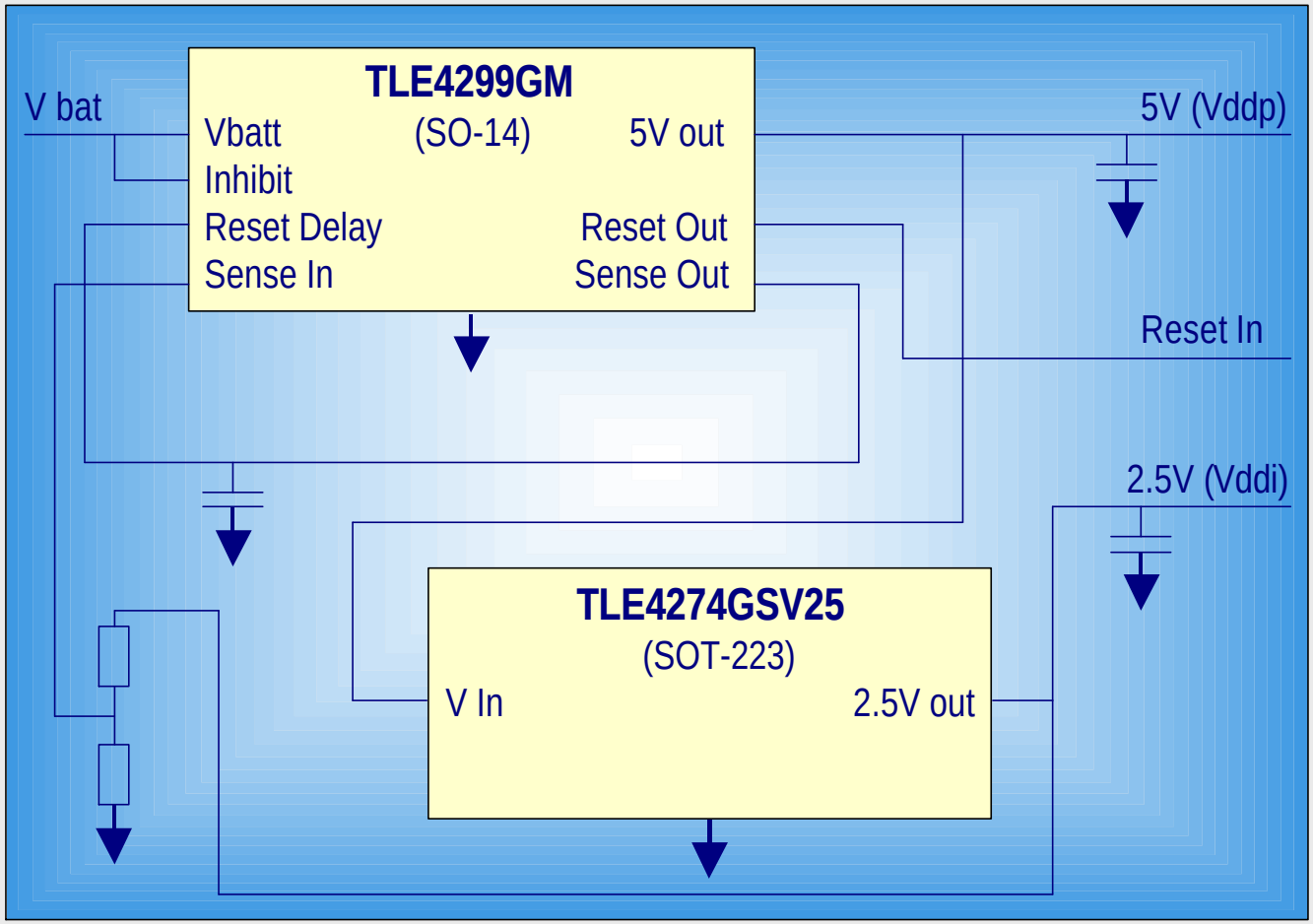
Note: V_{DD5V} = 4.5 V - 5.5 V ; $V_{DD2.5V}$ = 2.4 V - 2.7 V

Power Supply

- Reset Circuit
  - Reset must be held low until both power supplies have reached at least their respective minimum operating voltages:
    - Vddi = 2.4V
    - Vddp = 4.5V
  - Reset must remain low for at least 100ns to be reliably detected (from a XTAL running state)
  - Reset should remain low for at least 50ms to allow XTAL and PLL start-up (from a XTAL not running state)
  - RSTIN pin no longer has a built in pull up resistor, so needs to be biased externally. (Contrary to existing documentation)

Power Supply

- Voltage Regulator and Reset Circuit Discrete Realisation



Voltage regulator TLE7469

- **Output 5V/220mA & 2.6V/200mA**
- **Ultra low quiescent current <55µA**
- **Stable with some 100nF**
- **Active power sequencing**
- **Window watchdog**
- **Output reverse current sink**
- **Early warning comparator**
- **Inhibit input**
- **Very low drop voltage**
- **P-DSO-12**

Voltage regulator TLE7469

- Voltage Regulator and Reset Circuit Integrated Solution
  - Includes a windowed watchdog