Infineon technologies

Never stop thinking

XC166 architecture

TwinCAN

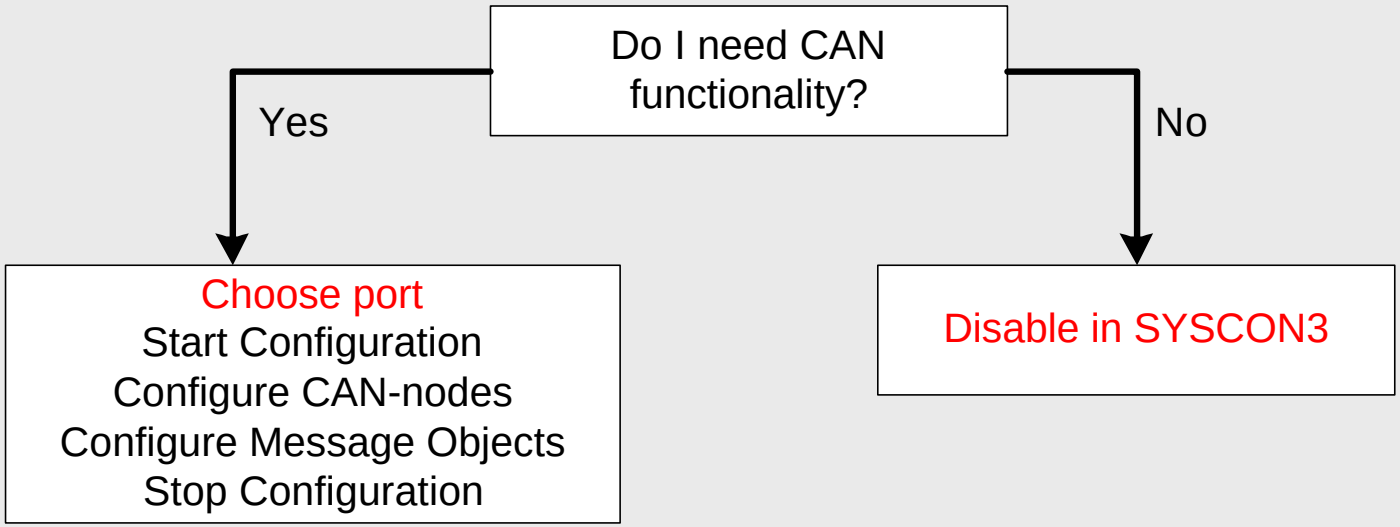
TwinCAN: basics

- Enabled after startup
- Assignable to port 4, (7) or 9.
- Compatible to 32bit module
- Difference to old 16bit CAN:
  - Additional node
  - More message objects
  - Mask on each message object
  - All message objects are receive/transmit configurable
  - FIFO/Gateway functionality

  Short: More features.

TwinCAN: getting started

Configurationflow



TwinCAN: configuration in short

- Choose port: Set CAN_PISEL, the corresponding ALTSEL register(s) and DPx.
- Start configuration: xCR := 0x41
- Configure the CAN nodes, like you need them
- Configure the message objects
- Stop configuration: CAN node not needed xCR:=1
  CAN node needed:
  xCR := $(0x00xxx00)_b$
- CAN action is able to start.

TwinCAN configuration of ports

- Choose port: Set CAN_PISEL, the corresponding ALTSEL register(s) and DPx.
  - CAN_PISEL configure the receive pins for the CAN.
  - ALTSELPx configure the port pin to be a special function pin.
  - DPx configure the direction of the port pin.

CAN_PISEL
TwinCAN Port Input Select Register — Reset Value: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										RISB			RISA		
r										rw			rw		

Field	Bits	Type	Description
RISA	[2:0]	rw	Receive Input Selection for Node A Bitfield RISA defines the input pin for the TwinCAN receive line RXDCA for node A. 000 The input pin for RXDCA is P4.5 001 The input pin for RXDCA is P4.7 010 The input pin for RXDCA is P7.6 011 The input pin for RXDCA is P9.2 1XX Reserved.
RISB	[5:3]	rw	Receive Input Selection for Node B Bitfield RISB defines the input pin for the TwinCAN receive line RXDCB for node B. 000 The input pin for RXDCB is P4.4 001 The input pin for RXDCB is P9.0 010 The input pin for RXDCB is P7.4 011 Reserved. 1XX Reserved.
0	[15:6]	r	reserved; returns '0' if read; should be written with '0';

ALTSEL0P4
P4 Alternate Select Register 0 — Reset Value: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								P7	P6	0					
r								rw	rw	r					

Field	Bit	Type	Description
ALTSEL0 P4.y	6, 7	rw	P4 Alternate Select Register 0 bit y 0 associated peripheral output is not selected as alternate function 1 associated peripheral output is selected as alternate function

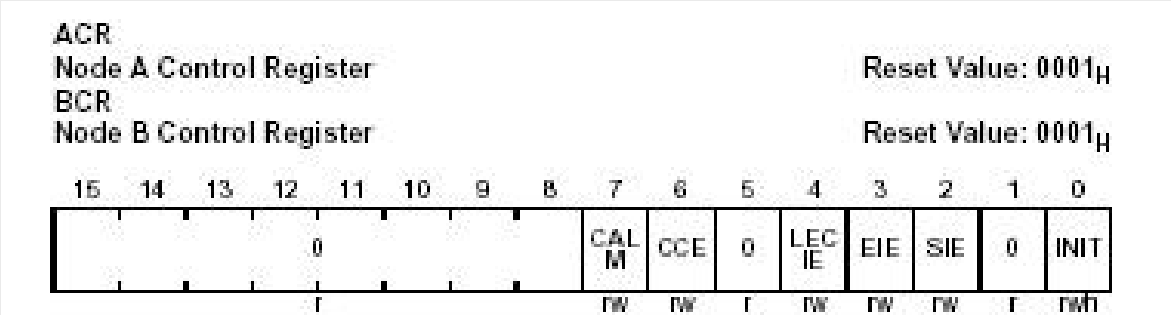
DP4
P4 Direction Ctrl. Register — Reset Value: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								P7	P6	P5	P4	P3	P2	P1	P0
r								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bit	Type	Description
DP4.y	[7:4]	rw	Port direction register DP4 bit y 0 Port line P4.y is an input (high-impedance) 1 Port line P4.y is an output

TwinCAN configure the nodes

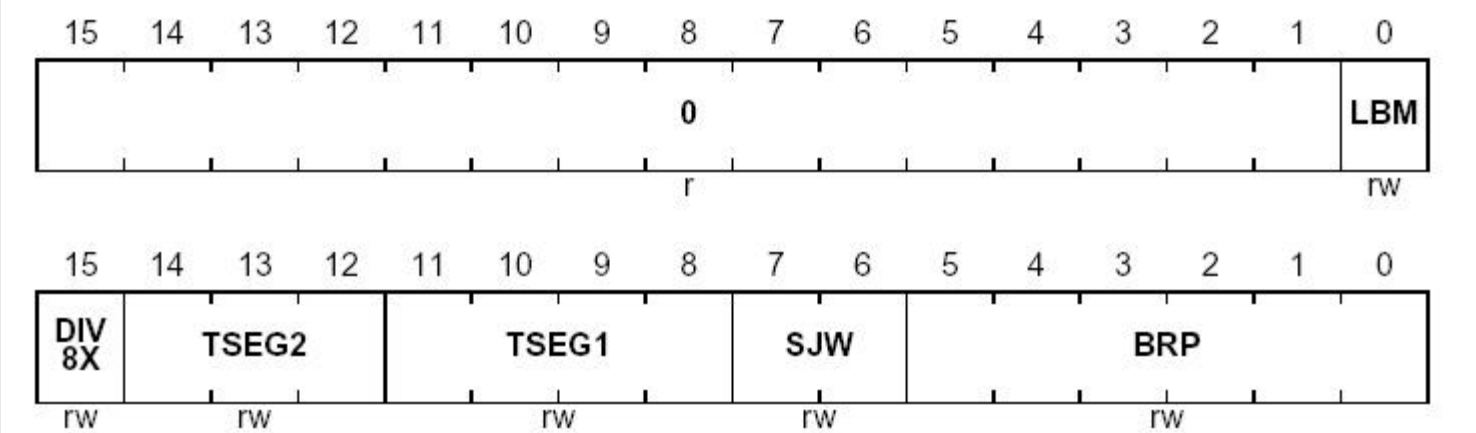
- Start configuration: xCR := 0x41
- Configure the CAN nodes, like you need them



  - CALM: Analyzer Mode, listening to the bus, receiving messages, but never answering
  - LECIE, EIE, SIE: status and error interrupts enable
  - CCE: Enable access to bittiming registers, disable modification of error counters.
  - INIT: Stops all CAN traffic, access to configuration registers is enabled, reset starts bus synchronization procedure.

TwinCAN, configure the nodes

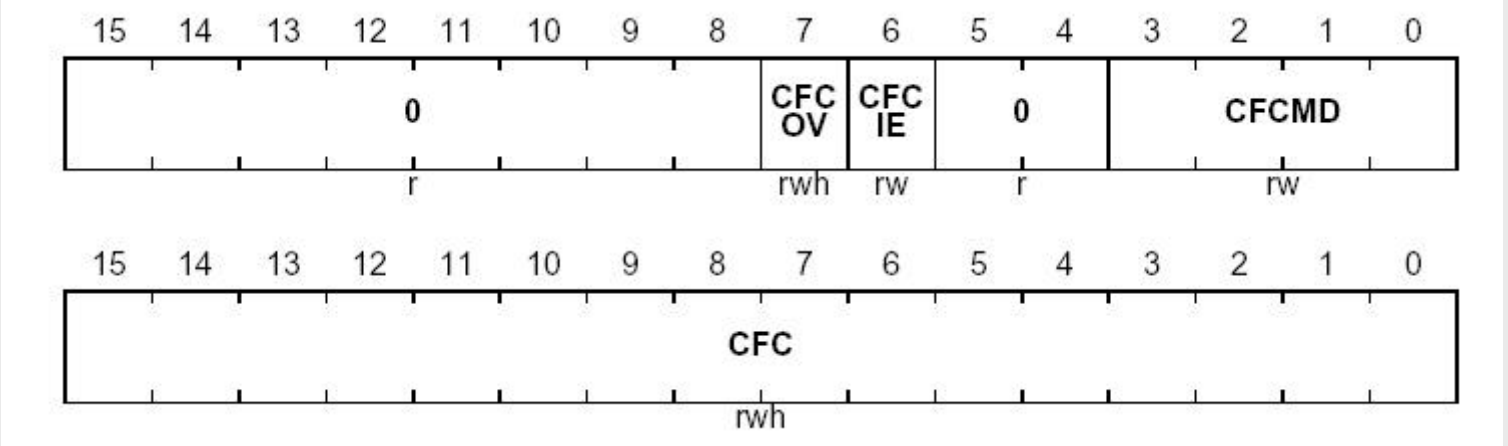
- Bittiming register xBTRH/L



  - LBM: Loop Back Mode (Internal connection, no outside signal)
  - DIV8x: Additional Divider of 8 for f_{CAN}
  - TSEG2, TSEG1, SJW: Define Sampling Point
  - BRP: Baudrate Prescaler

TwinCAN, configure the nodes

- Configure the Frame Counter xFCRH/L



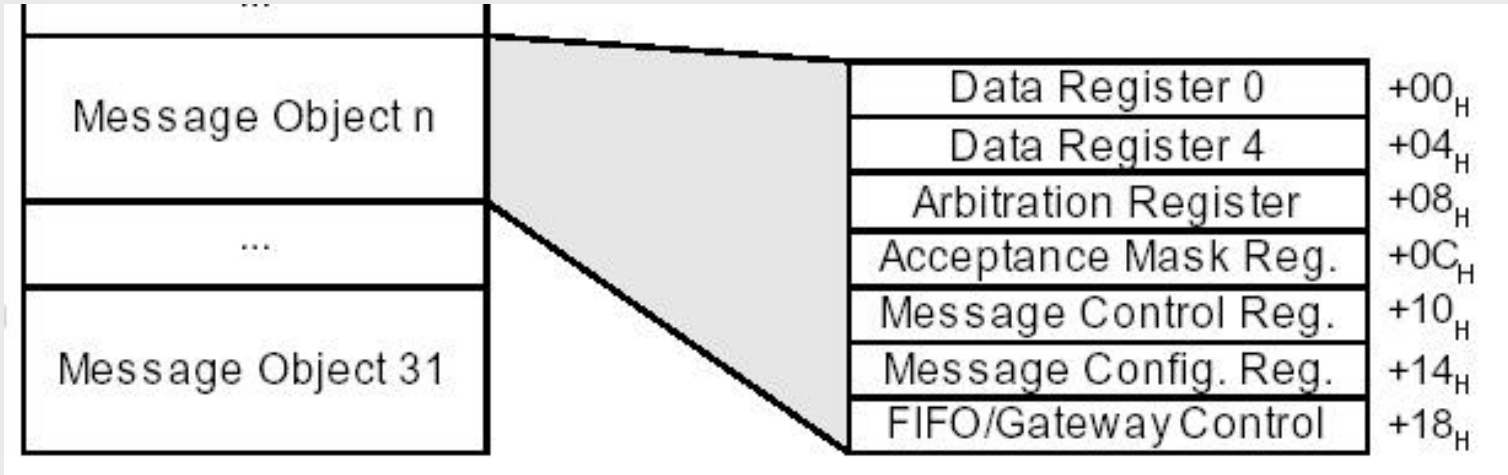
  - Interesting for analyzing purposes or time stamp systems
  - CFCMD: Frame Counter Mode
  - CFCOV/CFCIE: In case of overflow, define action

TwinCAN, configure the nodes

- Interrupt characteristics and reaction
  - xGINP: Which interrupt is related for which node
    - Define Interrupt Characteristics concerning node interrupt source numbers
  - xIMRH/L0/4: Interrupt Mask Register for message objects
    - Define the message objects, where an interrupt shell get through or not

TwinCAN, configure the message objects.

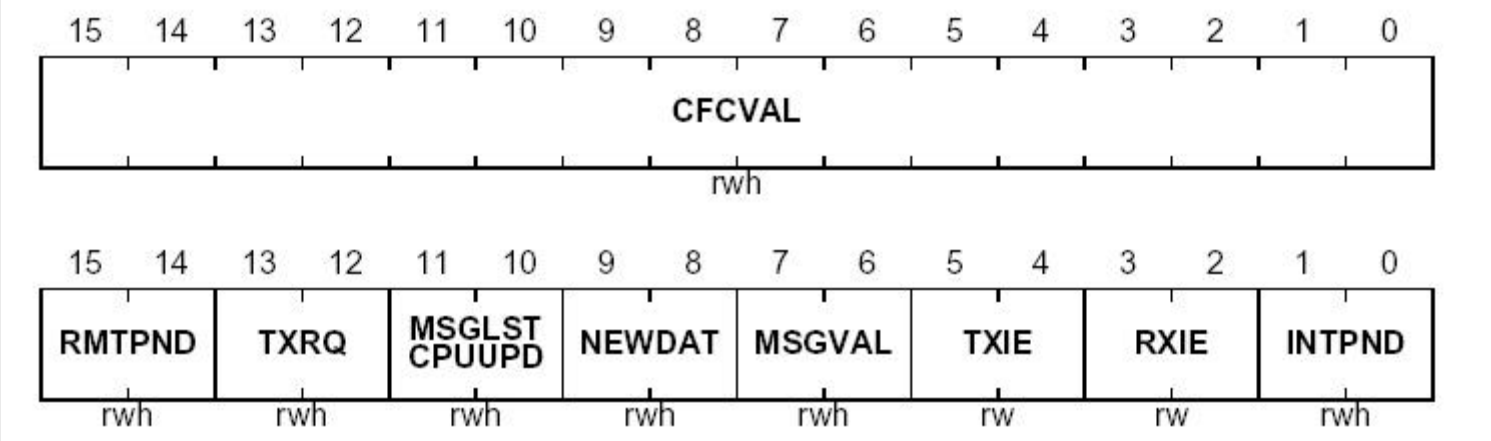
- Message Object Overview



  - MSGDRH/Lx0/4: Data Registers
  - MSGARH/Lx: Arbitration Register containing the message identifier
  - MSGAMRH/Lx: Arbitration Mask, 1 means, that the bit in the ID is taken into account for acceptance, 0 otherwise.

TwinCAN, configure the message objects.

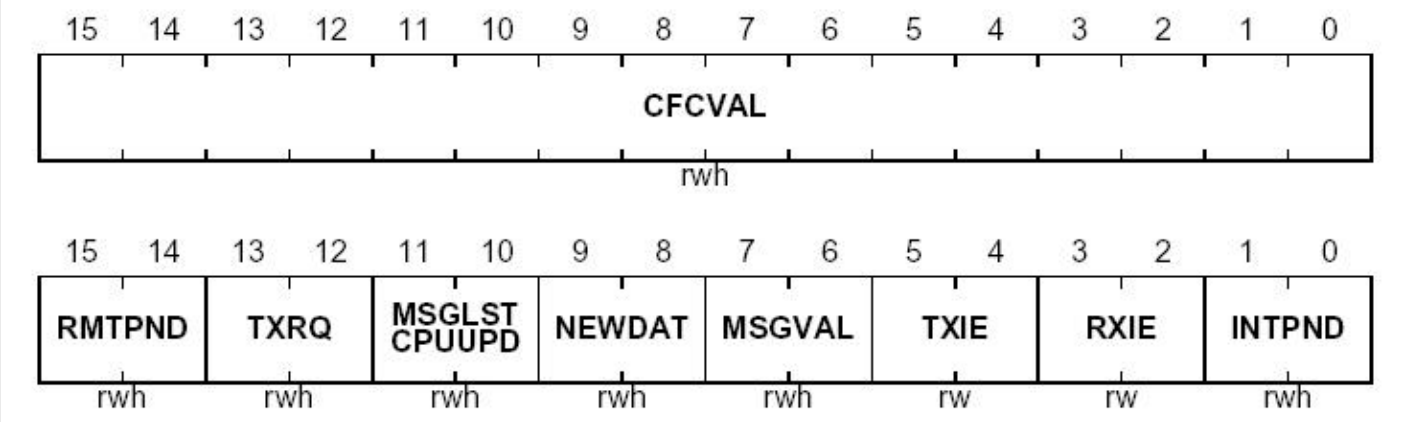
– MSGCTRH/Ln: Message Control Register



- INTPND: Interrupt Pending, shows if an interrupt is pending for this message object (reset by software!). Slow update!
- RXIE/TXIE: Define interrupt enable
- Tag message object to be valid or unvalid for changes. Set in order to take into account an update of bits XTD, DIR, NODE and CANPTR.

TwinCAN, configure the message objects.

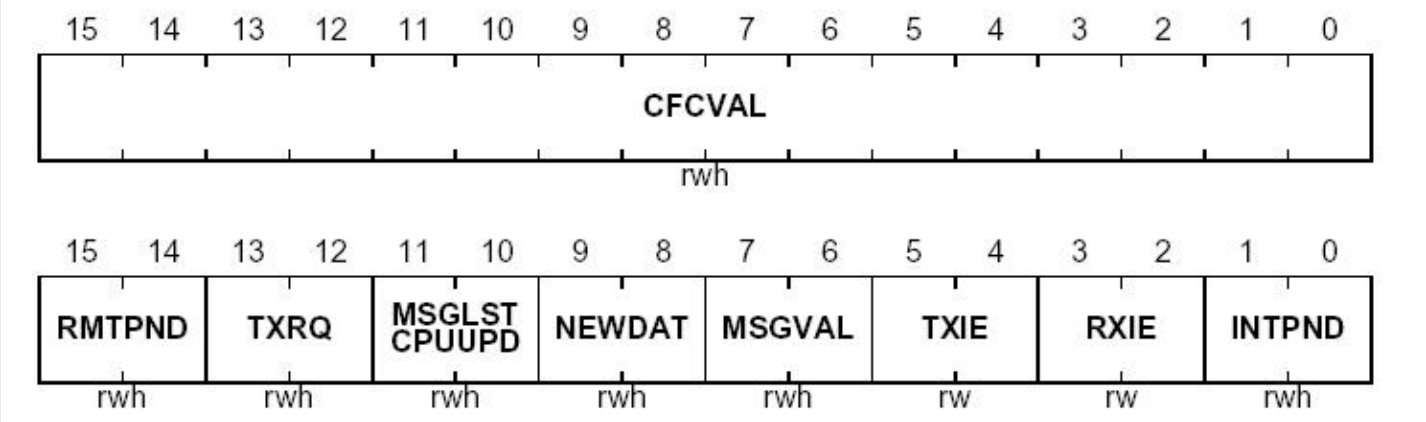
– MSGCTRH/Ln: Message Control Register



- NEWDAT:
  For Tx-Objects, this bitfield is supposed to be set by software. It indicates, that the contents is ready for sending and needs to be set to allow the message, to be copied into the bitstream.
  For Rx-Objects, this bitfield is set by hardware, to indicate, that a message has been received. This bit has to be reset by software. In case this bitfield is still set on NEWDAT and an additional message comes in for this object, a message loss will be indicated.

TwinCAN, configure the message objects.

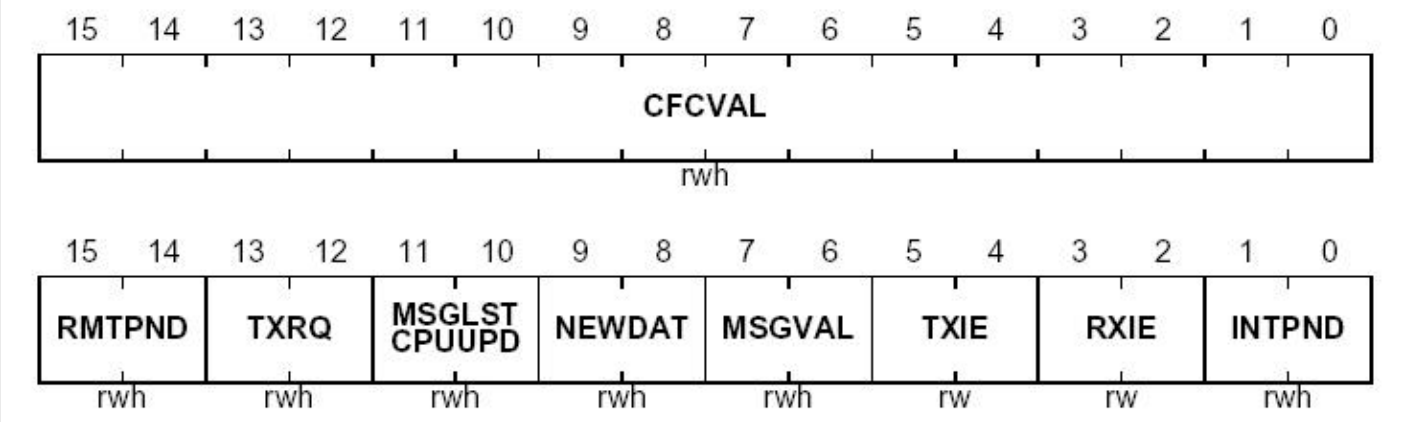
– MSGCTRH/Ln: Message Control Register



- MSGLST/CPUUPD:
  MSGLST: Indicates, that a new message has been received during NEWDAT is still set for this message object. This bit has to be reset by software.
  CPUUPD: This bit shall be set by software, to indicate, that transmission is forbidden, due to current changes on the message object.

TwinCAN, configure the message objects.

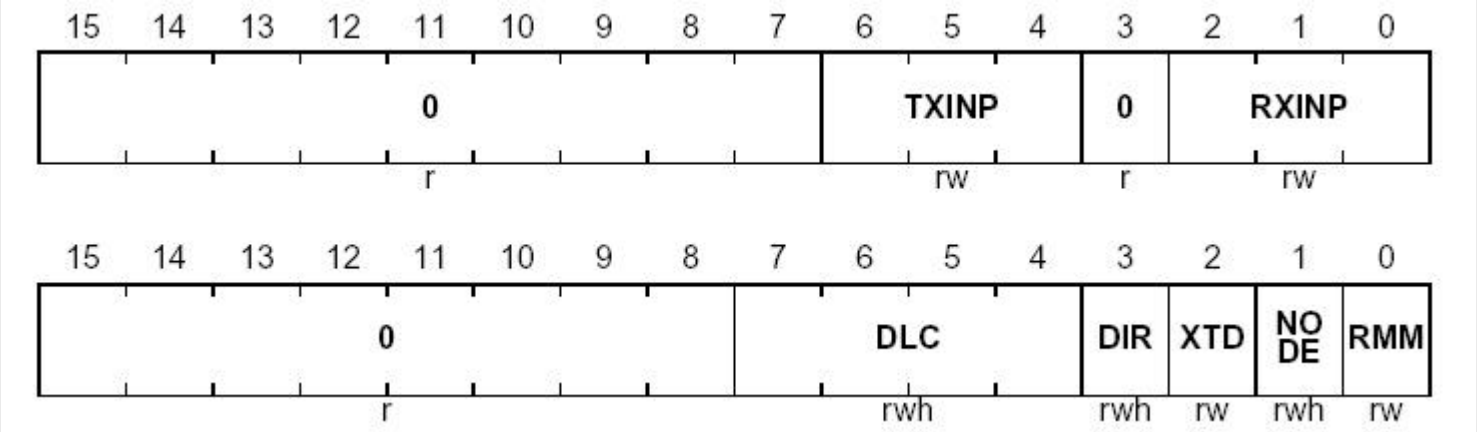
– MSGCTRH/Ln: Message Control Register



- TxRQ: Message is ready for transmission.
- RMTPND: Set for transmission objects, in case a remote request is still pending. TxRQ will be set as well.
- **General remark:** On this message object no direct move takes place. All bits will be changed by a logical bitwise AND.

TwinCAN, configure the message objects.

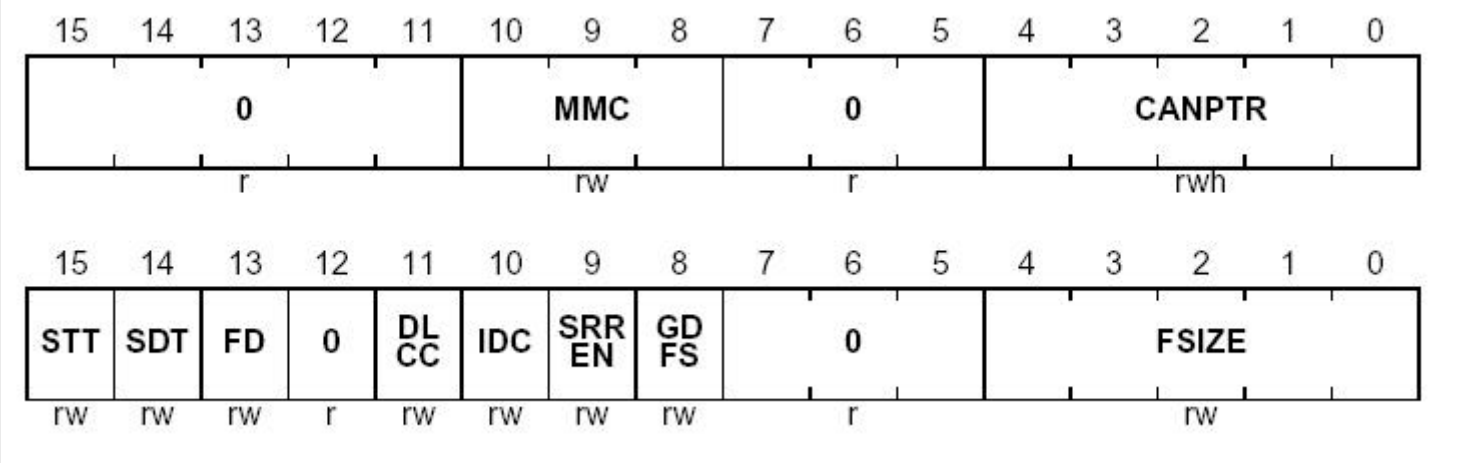
– MSGCFGH/Lx: Message Configuration Register



- RMM: Remote Monitoring Enable, in case the the identifier and the number of data bytes are copied into the remote frame. Only valid for transmit objects.
- NODE: Message object belongs to node A or B.
- XTD and DLC: Characteristics of message
- DIR: Receive or Transmit Object.
- RXINP, TXINP: Interrupt Source linked to this message object.

TwinCAN, configure the message objects.

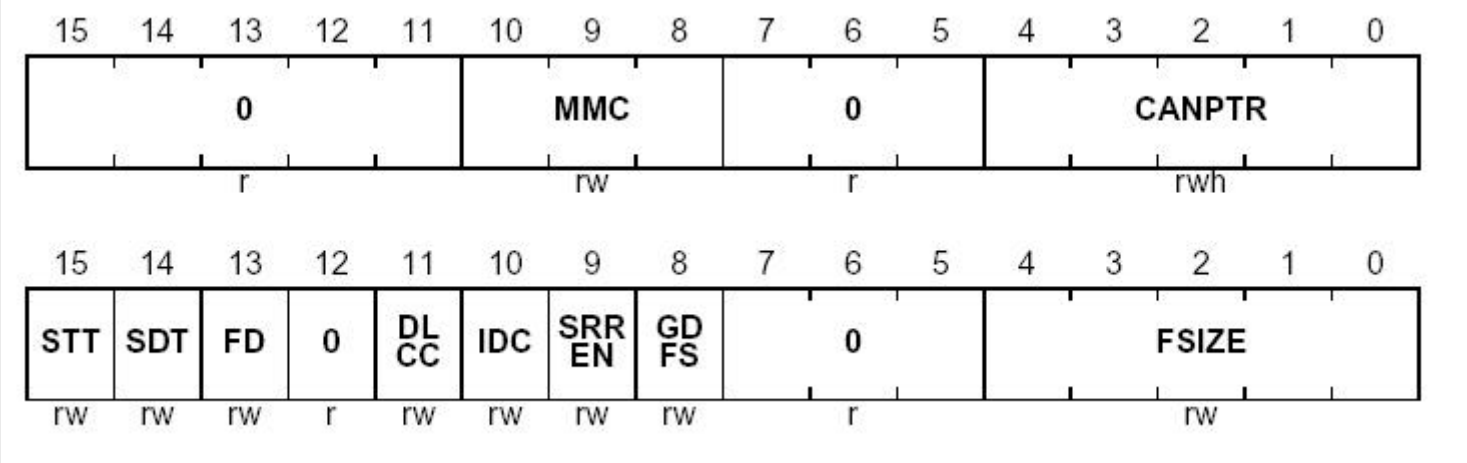
– MSGFGCRH/Lx: FIFO/Gateway Control Register



– MMC: Message Object Mode Control
Bitfield MMC controls the functionality of message object x. The user can choose between standard message object, FIFO (depending on the function and the position base or slave), normal gateway or shared gateway (receive side - depending on the position).

TwinCAN, configure the message objects.

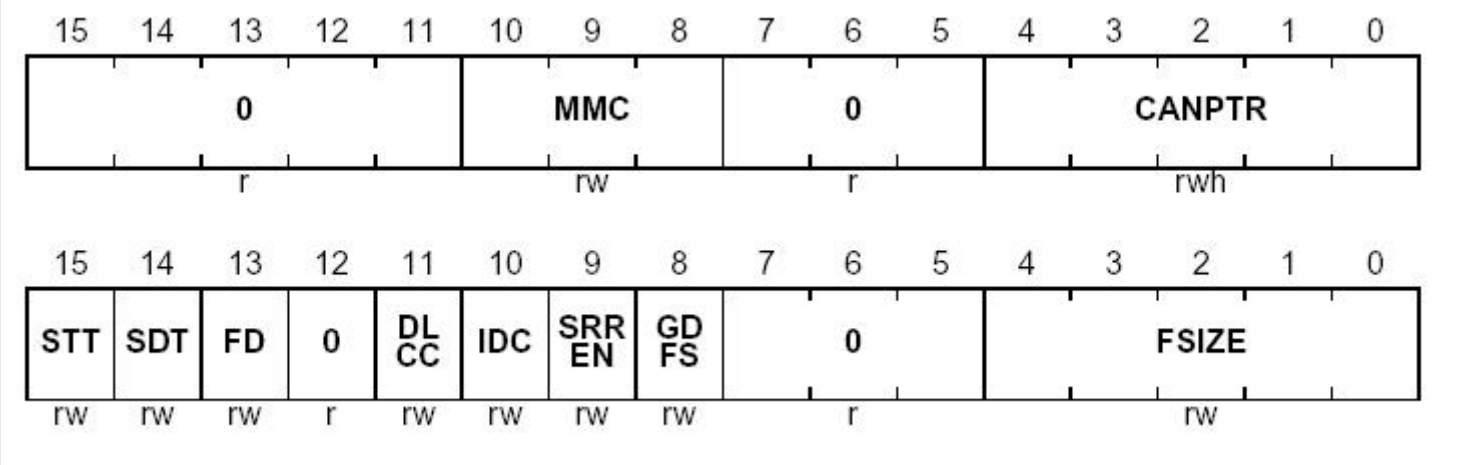
– MSGFGCRH/Lx: FIFO/Gateway Control Register



- CANPTR: CAN Pointer for FIFO/Gateway Functions depending on the value in MMC. In case an invalid or a wrong value is set in this register, no FIFO or normal gateway will work!
- SDT/STT: One shot modes. SDT, MSGVAL will be reset in case of bit set. STT, no automatic retransmission will take place.

TwinCAN, configure the message objects.

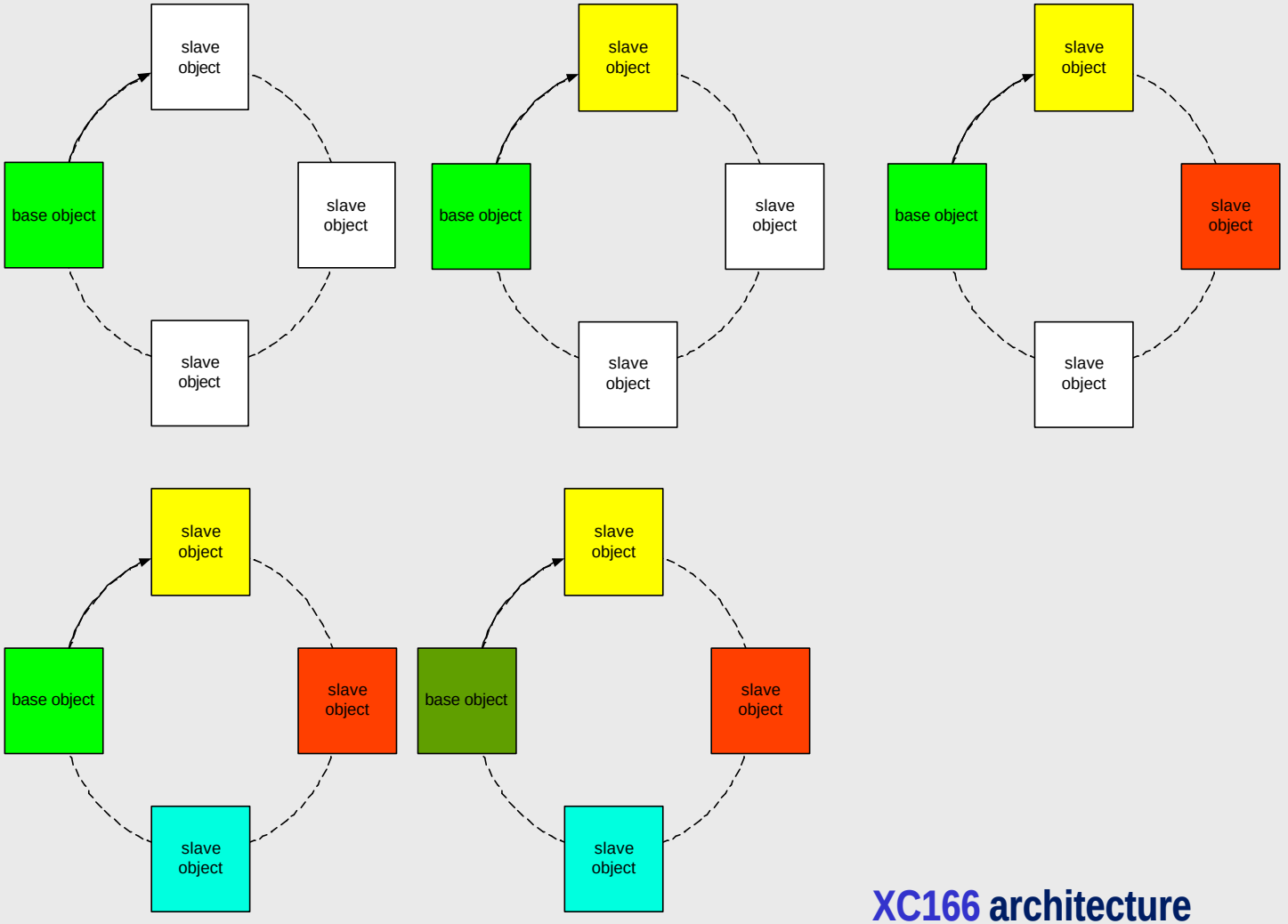
– MSGFGCRH/Lx: FIFO/Gateway Control Register



- FD: FIFO direction, defines update event of FIFO.
- IDC: Copy identifier in case of gateway function to the destination bus.
- SRREN: Remote requests pass the gateway.
- GDFS: Gateway function is complete done by hardware.
- FSIZE: length of FIFO.

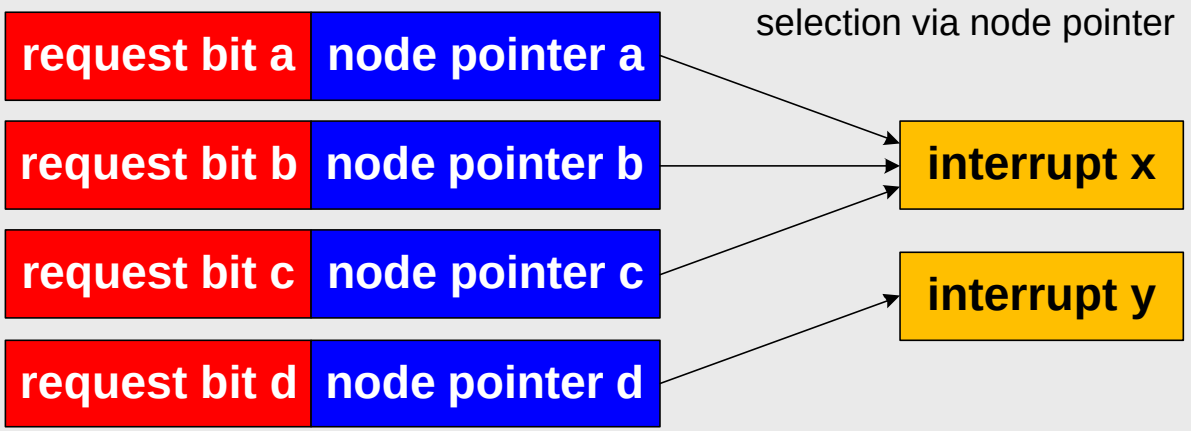
TwinCAN, configure the message objects.

- Filling the FIFO buffer



TwinCAN, Interrupts

- Up to eight individually programmable interrupt nodes can be used.
- 32 interrupts assignable to message objects of node A as well as to B plus four interrupt sources for each node.
- Concept:



- Do not use INTPND, use TXPND and RXPND!