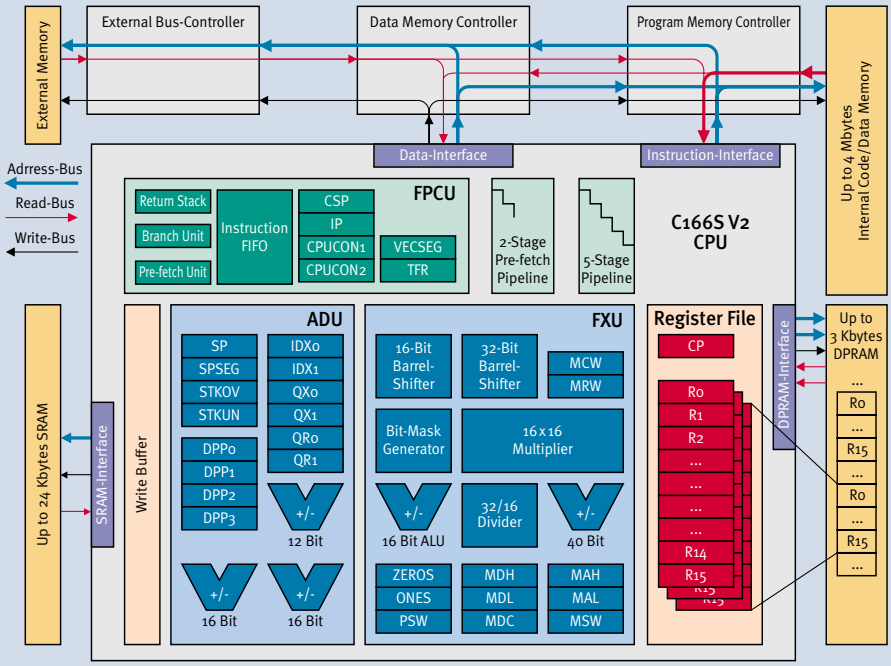
C166S V2

HIGHLIGHTS

C166S V2 is the most recent generation of the popular C166 microcontroller families. It combines high performance with enhanced modular architecture. Impressive DSP performance and advanced interrupt handling with fast context switching make C166S V2 the instrument of choice for powerful applications.

The system architecture inherits successful hardware and software concepts that have been established in the C166 16-Bit microcontroller families. C166 code compatibility enable re-use of existing code with optimized DSP support. This dramatically reduces the time-to-market for new product developments.

Debugging is supported with the OCDS (Level 1) block, which is supported by several emulator manufacturers. A bondout chip is available for building emulators.



Features

- 5-stage execution pipeline
- 2-stage instruction fetch pipeline with FIFO for instruction pre-fetching
- Pipeline with forwarding that controls data dependencies in hardware
- Flexible PMU and DMU with cache capabilities
- Multiple high bandwidth internal busses for data and instructions
- 16 Mbyte total linear address space
- 5 ns instruction cycle time at 200 MHz CPU clock, with nearly all instructions executed in one CPU clock cycle
- Enhanced boolean bit manipulation facilities
- Zero cycle jump execution
- Additional instructions to support HLL and operating systems
- Register-based design with multiple variable register banks
- Two additional fast register banks
- General purpose register architecture
- 16 general-purpose registers (GPRs) for byte and integer operands each
- Up to 128 interrupt's (including 2 fast interrupts)
- highly configurable system bus controller

Benefits

- Single clock cycle execution doubles the performance at the same CPU frequency (relative to the performance of the C166). Built-in advanced MAC unit dramatically increases DSP performance
- High Internal Program Memory bandwidth and the instruction fetch pipeline significantly improve program flow regularity and optimize fetches into the execution pipeline
- Sophisticated Data Memory structure and multiple high-speed data buses provide transparent data access (0 cycles) and broad bandwidth for efficient DSP processing
- Advanced exceptions handling block with multi-stage arbitration capability yields stellar interrupt performance with extremely small latency

Infineon technologies

Never stop thinking.