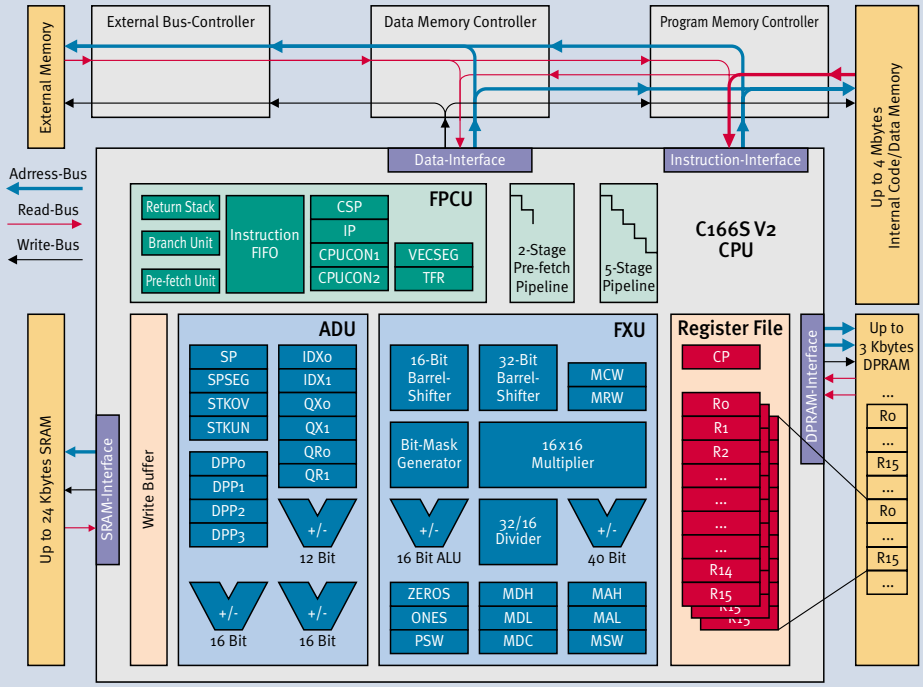
C166S V2

HIGHLIGHTS

C166S V2 is the most recent generation of the popular C166 microcontroller families. It combines high performance with enhanced modular architecture. Impressive DSP performance and advanced interrupt handling with fast context switching make C166S V2 the instrument of choice for powerful applications.

The system architecture inherits successful hardware and software concepts that have been established in the C166 16-Bit microcontroller families. C166 code compatibility enable re-use of existing code with optimized DSP support. This dramatically reduces the time-to-market for new product developments.

Debugging is supported with the OCDS (Level 1) block, which is supported by several emulator manufacturers. A bondout chip is available for building emulators.



Features

- 5-stage execution pipeline
- 2-stage instruction fetch pipeline with FIFO for instruction pre-fetching
- Pipeline with forwarding that controls data dependencies in hardware
- Flexible PMU and DMU with cache capabilities
- Multiple high bandwidth internal busses for data and instructions
- 16 Mbyte total linear address space
- 5 ns instruction cycle time at 200 MHz CPU clock, with nearly all instructions executed in one CPU clock cycle
- Enhanced boolean bit manipulation facilities
- Zero cycle jump execution
- Additional instructions to support HLL and operating systems
- Register-based design with multiple variable register banks
- Two additional fast register banks
- General purpose register architecture
- 16 general-purpose registers (GPRs) for byte and integer operands each
- Up to 128 interrupt's (including 2 fast interrupts)
- highly configurable system bus controller

Benefits

- Single clock cycle execution doubles the performance at the same CPU frequency (relative to the performance of the C166). Built-in advanced MAC unit dramatically increases DSP performance
- High Internal Program Memory bandwidth and the instruction fetch pipeline significantly improve program flow regularity and optimize fetches into the execution pipeline
- Sophisticated Data Memory structure and multiple high-speed data buses provide transparent data access (0 cycles) and broad bandwidth for efficient DSP processing
- Advanced exceptions handling block with multi-stage arbitration capability yields stellar interrupt performance with extremely small latency

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Description

CPU

- 5 ns instruction cycle time @ 200 MHz clock
- Register based design
- RTOS and HLL instructions
- 16 Mbyte linear address space
- 128 interrupts (inc. 2 fast interrupts)

Single cycle MAC

- 16x16-Bit multiplier
- 32-Bit barrel shifter
- 32/16-Bit divider

Multiple high bandwidth data bus systems

- 16-Bit high performance system bus (Ext. bus 8/16 Bit, muxed/demuxed, 8 configurable chip selects; X-Bus support)
- 16-Bit enhanced peripheral bus (PDBUS+)
- 64-Bit internal program memory bus (single cycle access)
- 16-Bit data memory bus (0 cycle access)

Debug

- JTAG
- OCDS Level 1
- Bondout chip available

Technical Data

- Synthesizable Core
- Silicon proven in 0.18 µm technology
- Supply voltage 1.8 V
- 0.9 mW/MHz with
  - CPU, PMU, DMU, EBC, IAI (32 nodes)
  - 512 Kbyte Code-SRAM, 8 Kbyte Data-SRAM, 2 Kbyte DPRAM
  - Port 2, 3, 5
  - Peripherals: SSC, ASC, GPT12, PWM
  - System control unit (SCU)
  - JTAG

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Product Brief

The C167CS* is a new high end derivative of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. The C167CS features additionally internal units like two CAN modules (V2.0B active), ADC, CAPCOM, XRAM, IRAM, PLL, Watchdog, RTC, GPT, power management control and up to 40 MHz performance. This microcontroller fulfills the requirements of highly sophisticated automotive and industrial control applications.

Device	ROM
C167CS-4RM	32 KB
C167CS-LM	–

25 MHz = standard
33 MHz = optional
40 MHz = optional
3.3V at 16 MHz = optional

KEY FEATURES

- High Performance 16-bit CPU with 4-Stage Pipeline
- 80 ns Instruction Cycle Time at 25 MHz CPU Clock (standard)
- Up to 12.5 million instructions per second
- 400 ns Multiplication (16 x 16 bit), 800 ns Division (32/16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via on-chip PLL or via Direct Clock Input
- Up to 16 MBytes Linear Address Space for Code and Data
- 3 KByte On-Chip Internal RAM (IRAM)
- 8 KByte On-Chip Extension RAM (XRAM)
- Two On-Chip CAN modules operating on one or two CAN Buses (30 or 2x15 Message Objects) Version 2.0B active
- Programmable External Bus Characteristics for Different Address Ranges
- 8-bit or 16-bit External Data Bus
- Multiplexed or Demultiplexed External Address/Data Buses
- Five Programmable Chip-Select Signals
- Hold and Hold-Acknowledge Bus Arbitration Support
- 1024 Byte On-Chip Special Function Register Area
- Idle, Power Down Modes and Power Saving Features
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40 ns
- 24-Channel 10-bit A/D Converter with <10µs Conversion Time (7.76 µs at 25 MHz)
- Two 16-Channel Capture/Compare Units with Bidirectional I/O Port Pins
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- Programmable Watchdog Timer
- Real Time Clock
- On-Chip Bootstrap Loader
- Oscillator Watchdog
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Identification Register Support
- Optimized EMC Behavior
- Exit/Wakeup from Sleep Mode with External Interrupt or RTC Interrupt
- Single Chip Reset (optional)
- Flexible CAN Interface Line Assignment for additional Address Pins (use Address Pins while CAN is active)
- Compatible in Pins, Timing and Code to existing C167CR Derivatives
- Supported by a Wealth of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers
- 144-Pin MQFP Package
- Full Automotive Temperature Range: –40°C to +125°C

Controller Area Network (CAN): License of Robert Bosch GmbH

* For complete device designations (corresponding to PRO ELECTRON please refer to the data sheet)

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C167CS

High Performance Microcontroller with On-chip Memory and TWO-CAN-Modules

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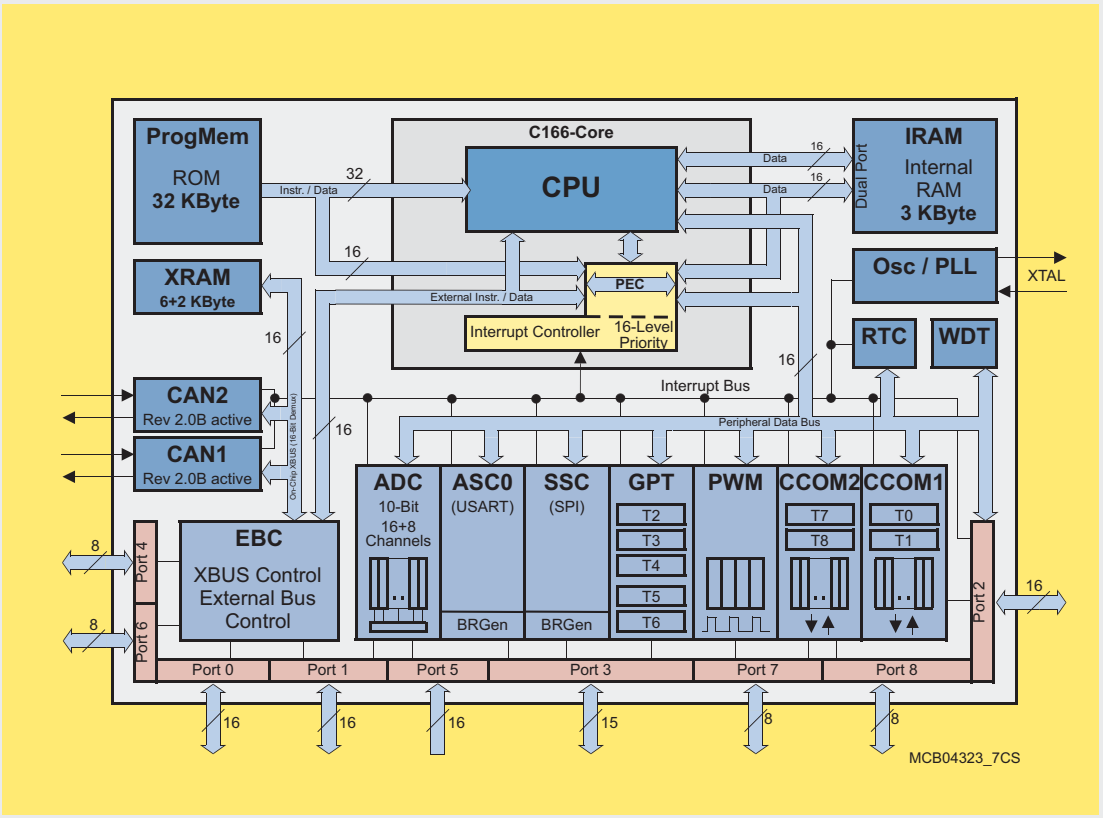
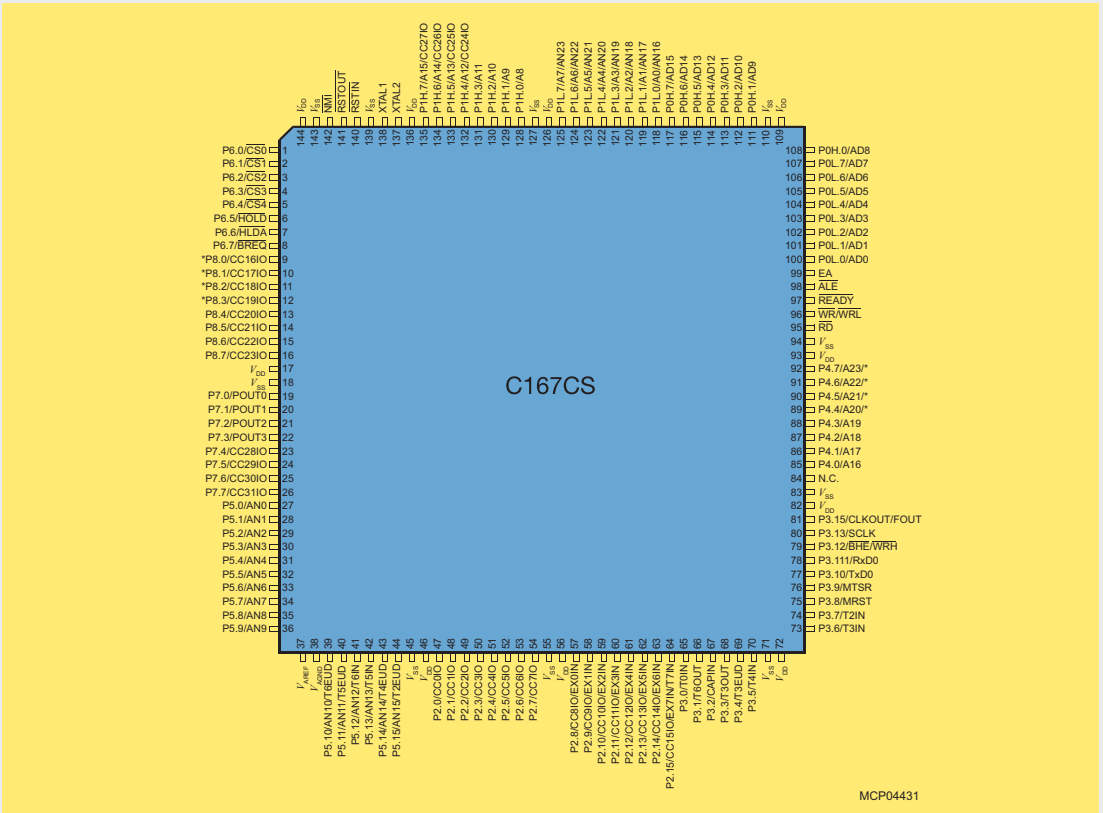
Never stop



C167CS: BLOCK DIAGRAM



C167CS: PIN CONFIGURATION

* The marked pins of port 4 and port 8 can have CAN Interface lines assigned to them

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